

Wistron-KBLU Schematics

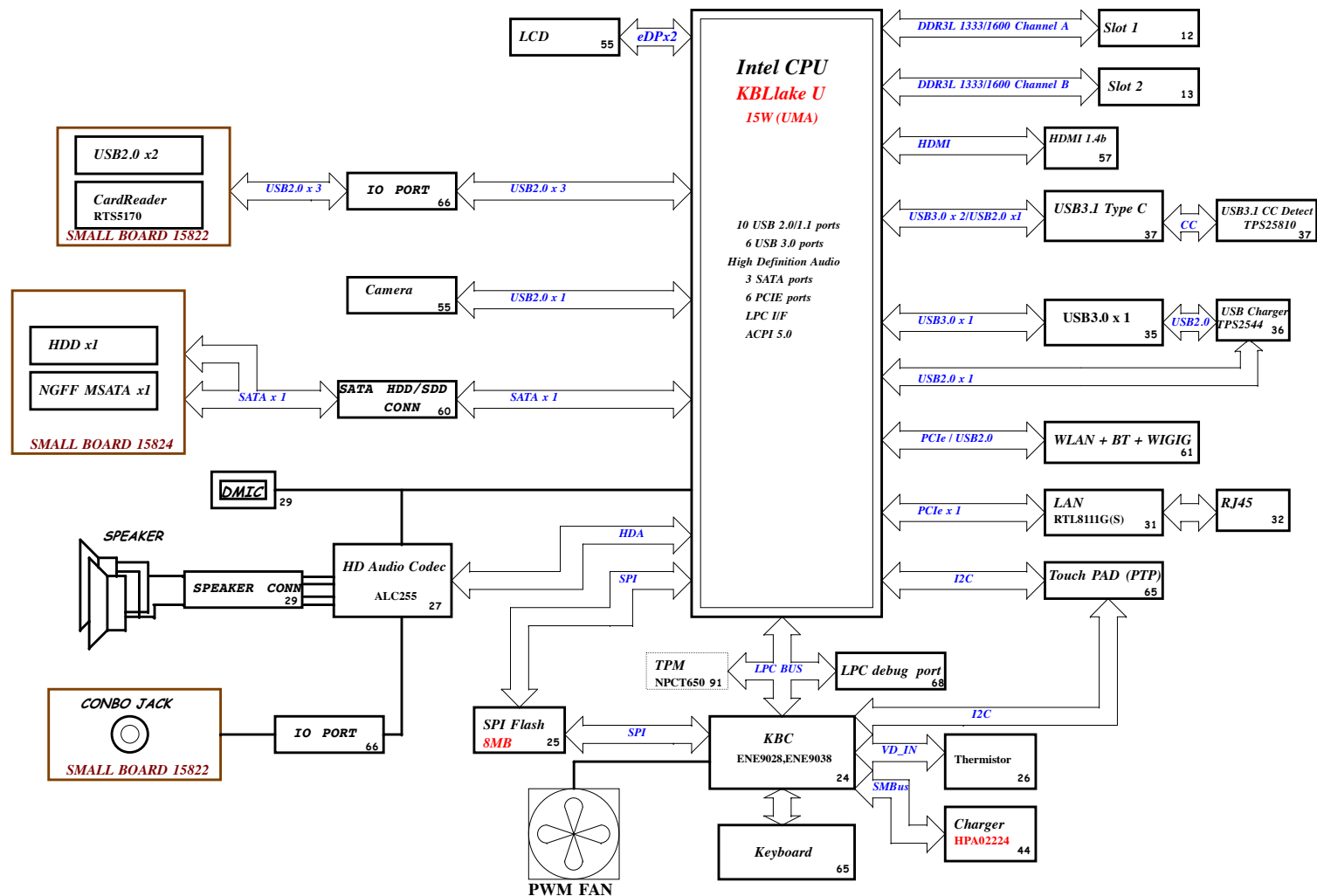
BA30

REV : -3

DY : None Installed

per MP	
<div>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title	
Cover Page	
Size A3	Document Number Mihawk MB
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Project code:
Mihawk SL 13 --> 4PD06J010001
PCB P/N:15208
Revision: -1

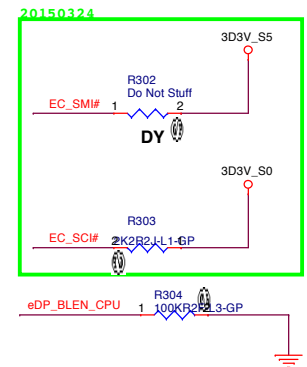


CHARGER		44
HPA02224		
INPUTS	OUTPUTS	
AD+	BT+	DCBATOUT
SYSTEM DC/DC		45
RT6575D		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5	
CPU Core Power		46
ISL95857HRTZ-T-GP		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DDR3L SUS		51
RT8231AGQW-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3 0D675V_S0	
CPU 1D0V_S5		52
RT8231AGQW-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	
CPU 1.8V_S5		53
RT8068AZQWID-GP-U		
INPUTS	OUTPUTS	
DCBATOUT	1D8V_S5	
Switches		40
INPUTS	OUTPUTS	
1D0V_S5	1D0V_EOPIO_EDRAM	
5V_S5	5V_S0	
3D3V_S5	3D3V_S0	
1D0V_S5	1V_VCCIO	
	1V_VCCSR	
PCB LAYER		
8-1.0-16d	L1:Top L2:GND L3:Signal L4:Signal L5:GND L6:Signal L7:GND L8:Bottom	

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Title			
Block Diagram			
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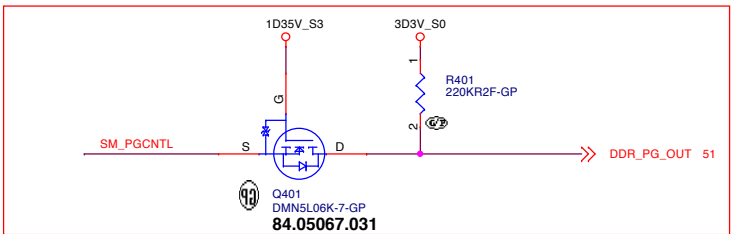
Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω \pm 5%	Max = 100 mils

Size
A3

DDR3L ball type: Interleaved Type



GP SKYLAKE-U-GP



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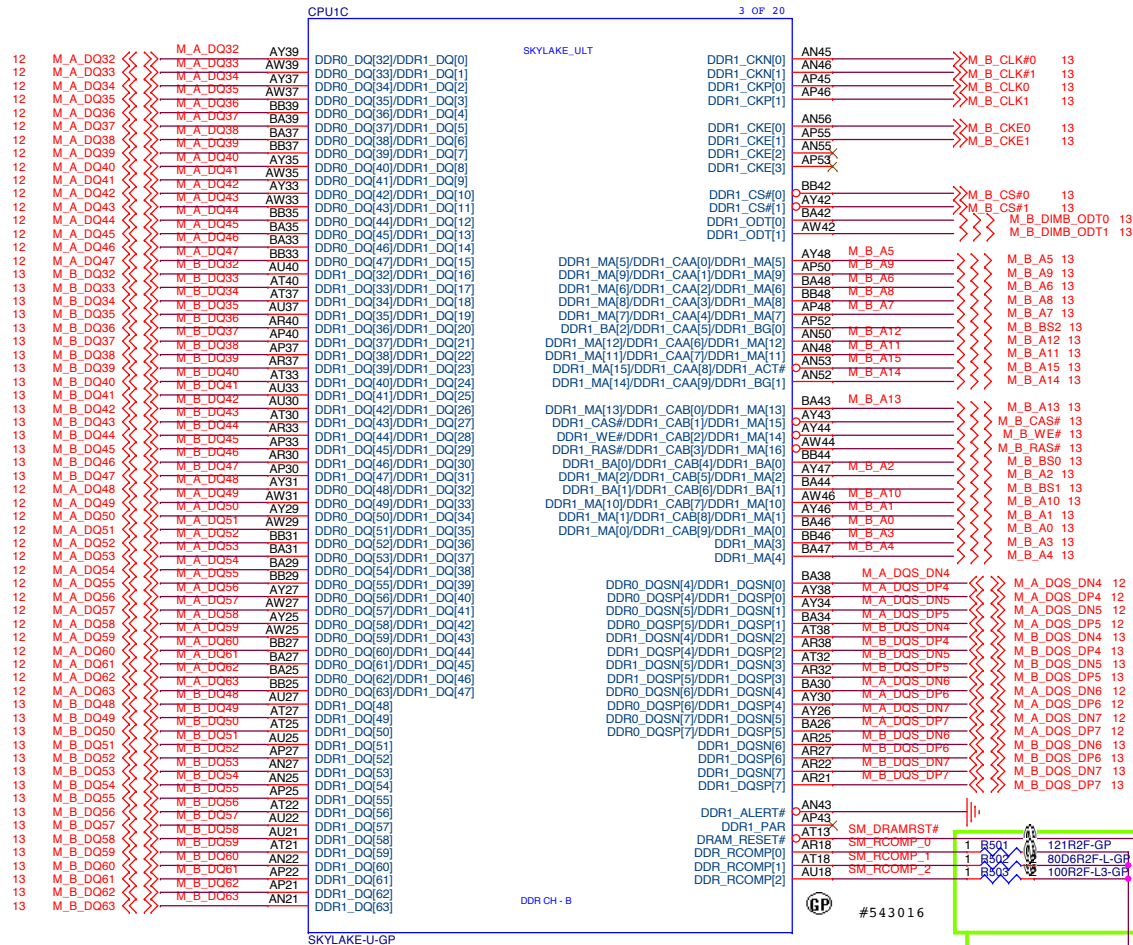
CPU_(DDR)

Mihawk MB

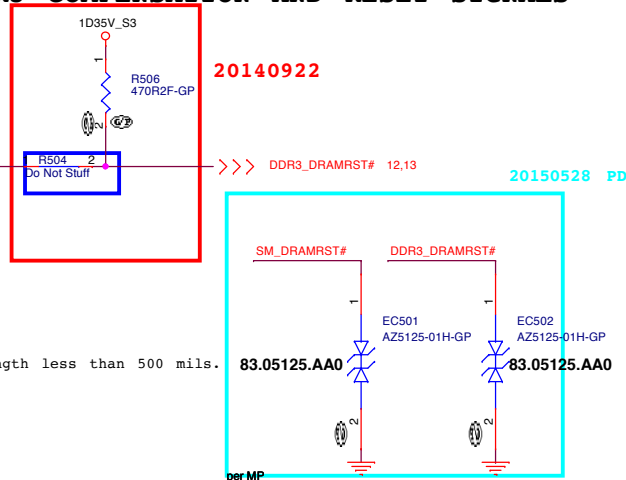
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Main Func = CPU



DDR3 COMPENSATION AND RESET SIGNALS

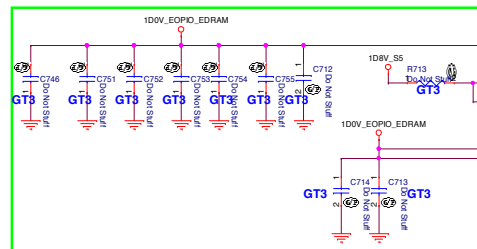


Layout Note:
Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

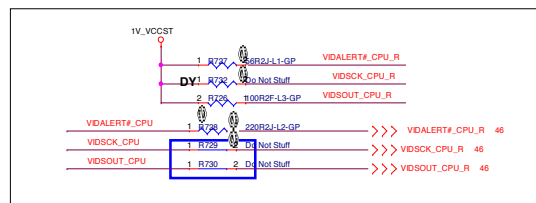
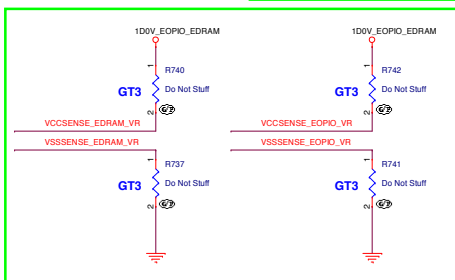
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Title			
CPU (LPSS/ISH)			
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20150320



20150319



CLOSE CPU

SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

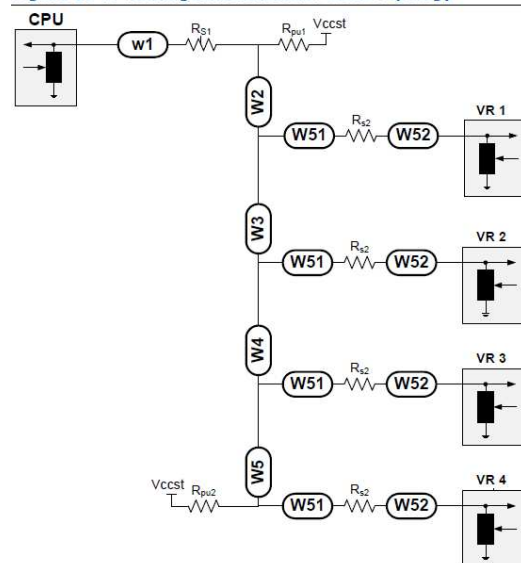
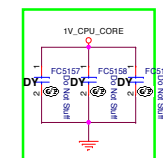


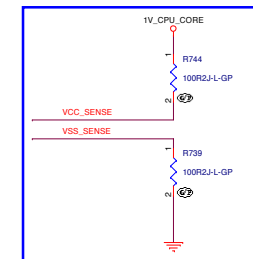
Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R _{PU1} [Ω]	R _{PU2} [Ω]	R _{S1} [Ω]	R _{S2} [Ω]	V _{CCST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

20150322



20150505 SB

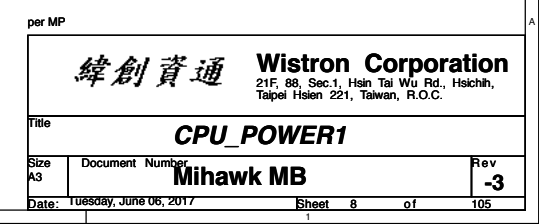


Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE Impedance<50 ohm
3. Length match<25mil

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Main Func = PCH

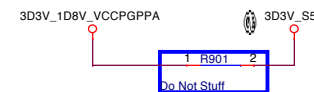
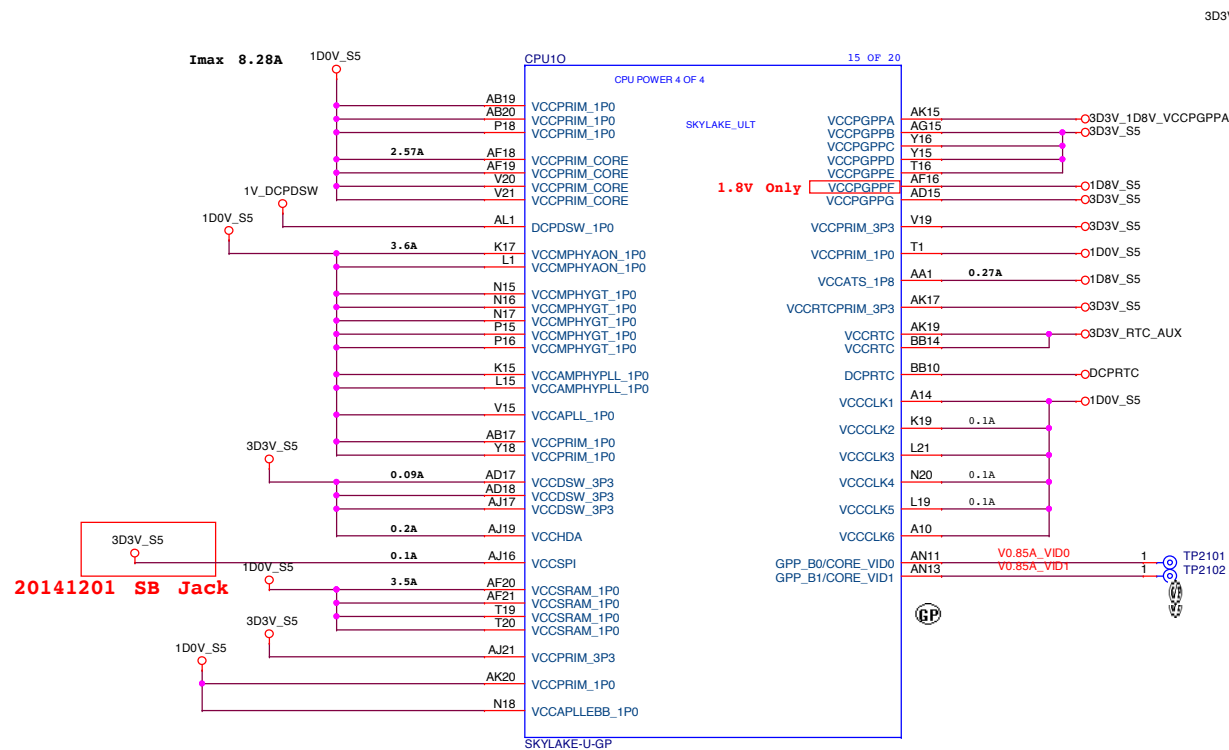
**eSPI_508740:**

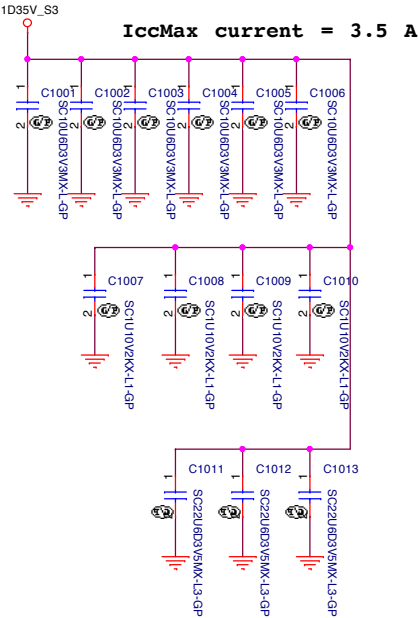
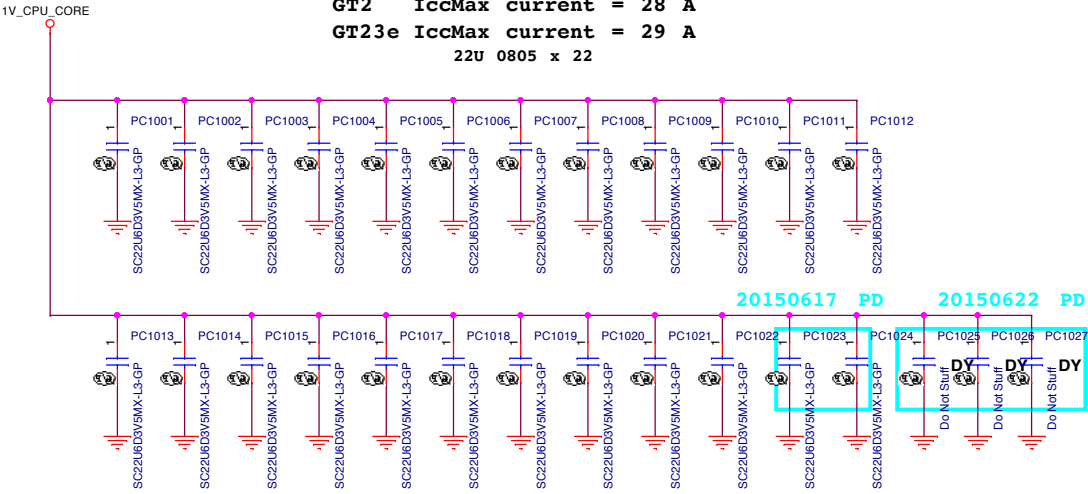
Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SM LOALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

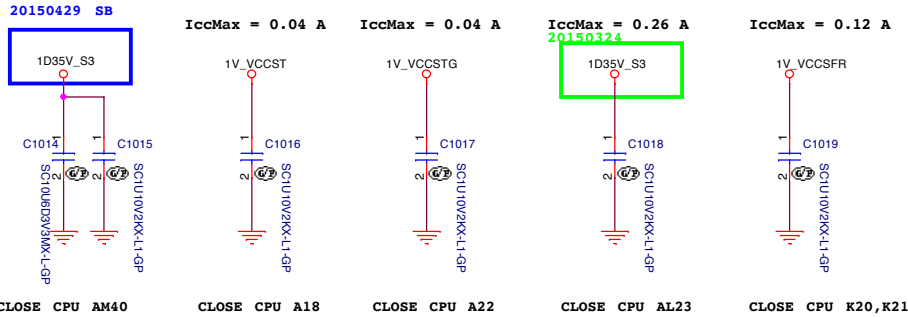
Main Func = CPU

GT2 IccMax current = 28 A
GT23e IccMax current = 29 A
22U 0805 x 22



U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
	GT	750KHz	40A (31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF

V _{DDQ}	2x 10 uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1 uF 0201 (Placeholder)		
		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible



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CPU_(Power CAP1)

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Main Func = CPU

1V_VCCGT

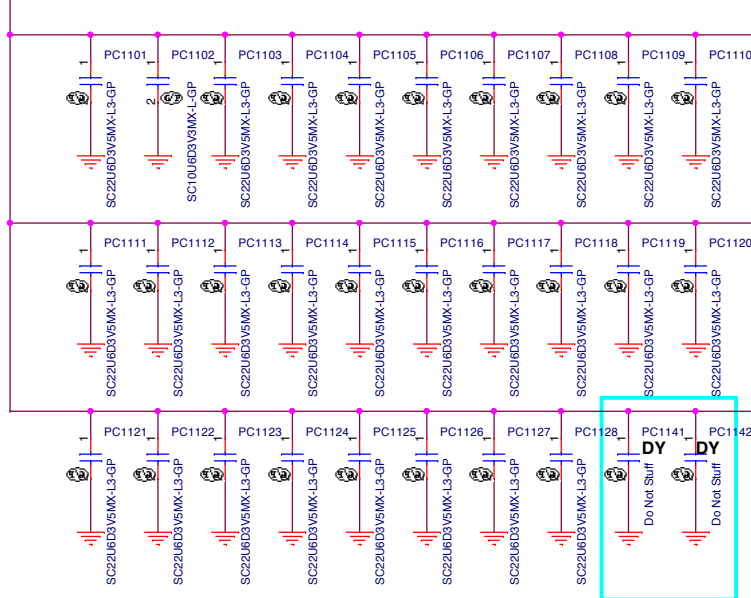
GT

GT2

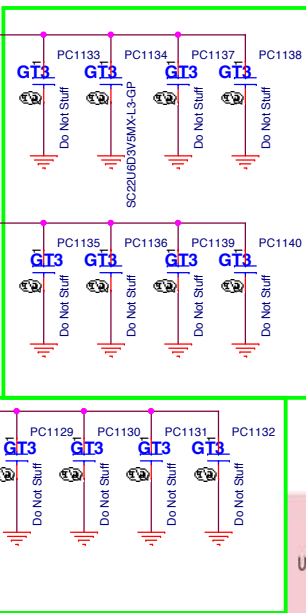
IccMax current = 31 A

GT23e

IccMax current = 64 A



20150617 PD



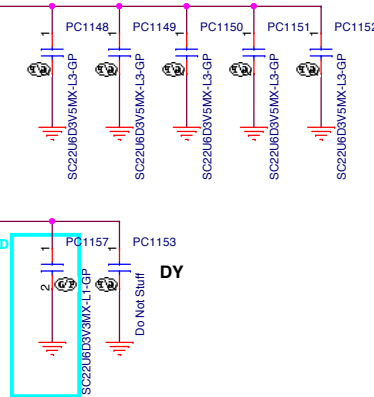
1V_VCCSA

VCCSA

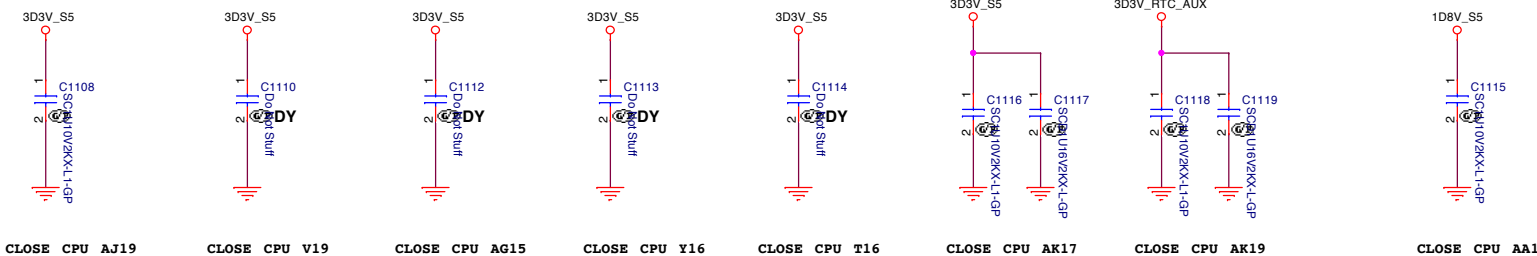
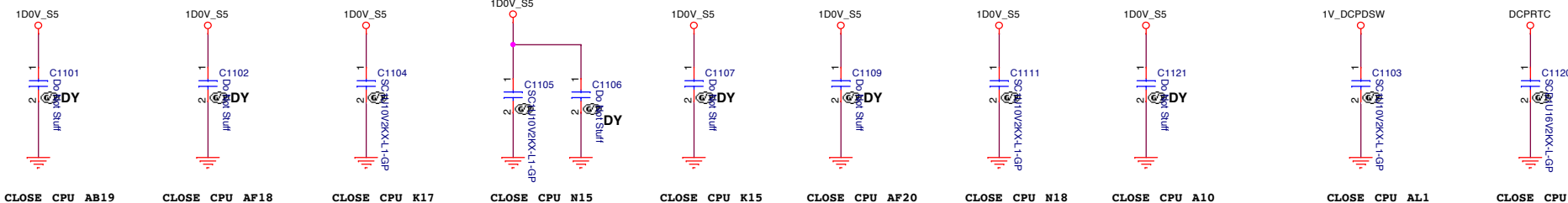
ICCMAX.=7A

20150617 PD

DY



U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF



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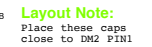
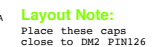
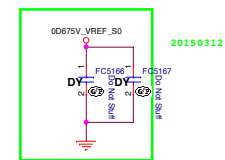
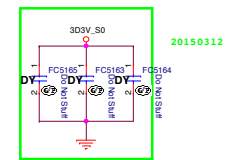
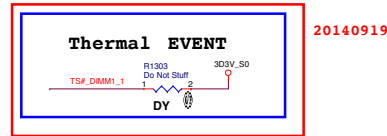
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Title CPU_(Power CAP2)

Size A3 Document Number Mihawk MB Rev -3

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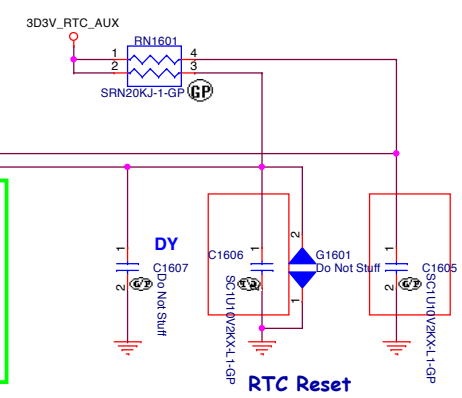
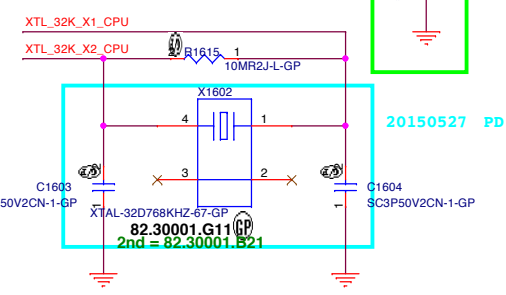
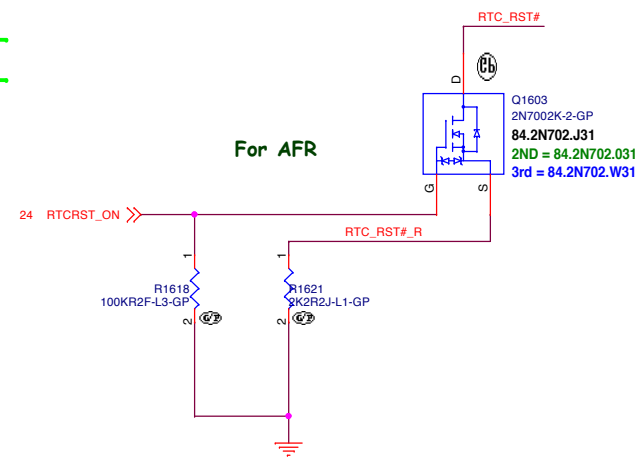
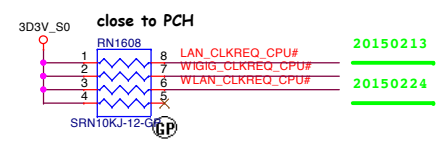
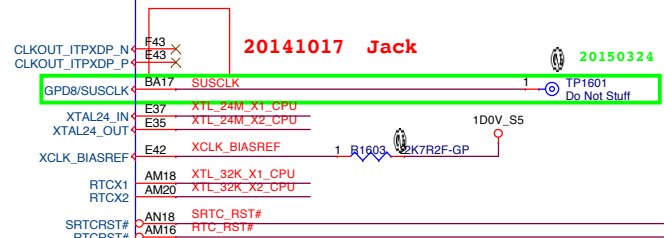
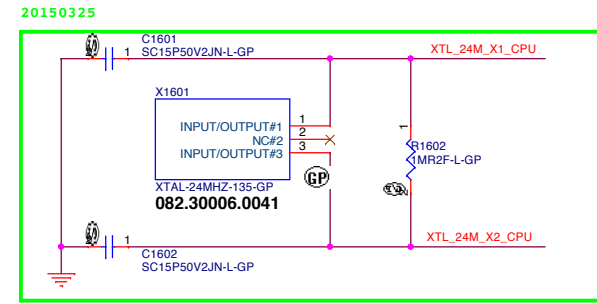
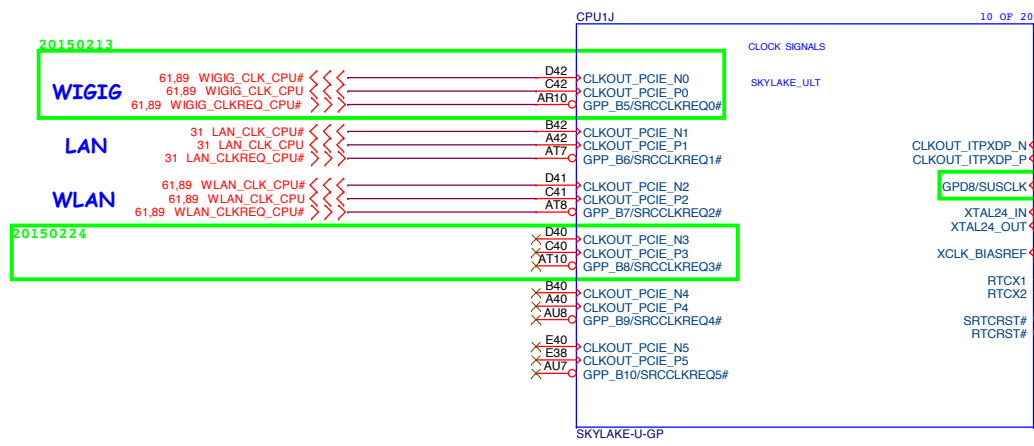


SSID = STRAP

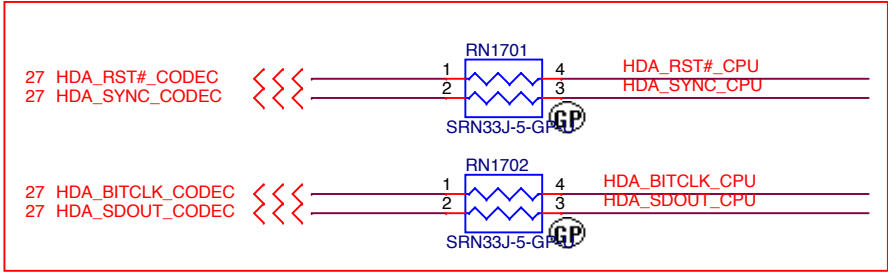
STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected		Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected		Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

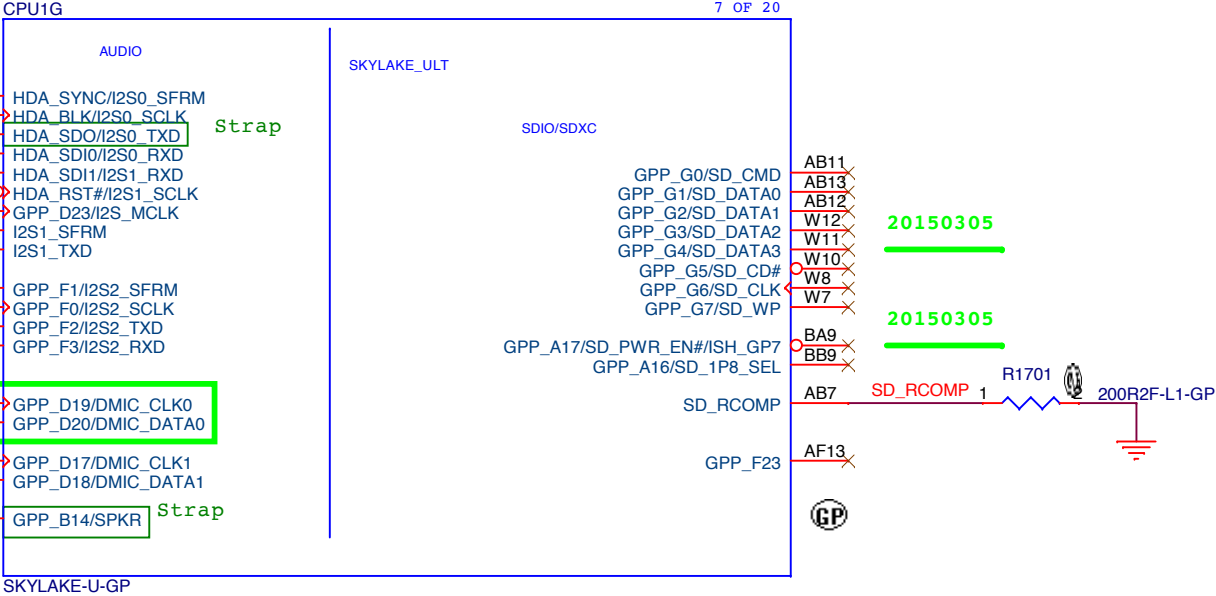
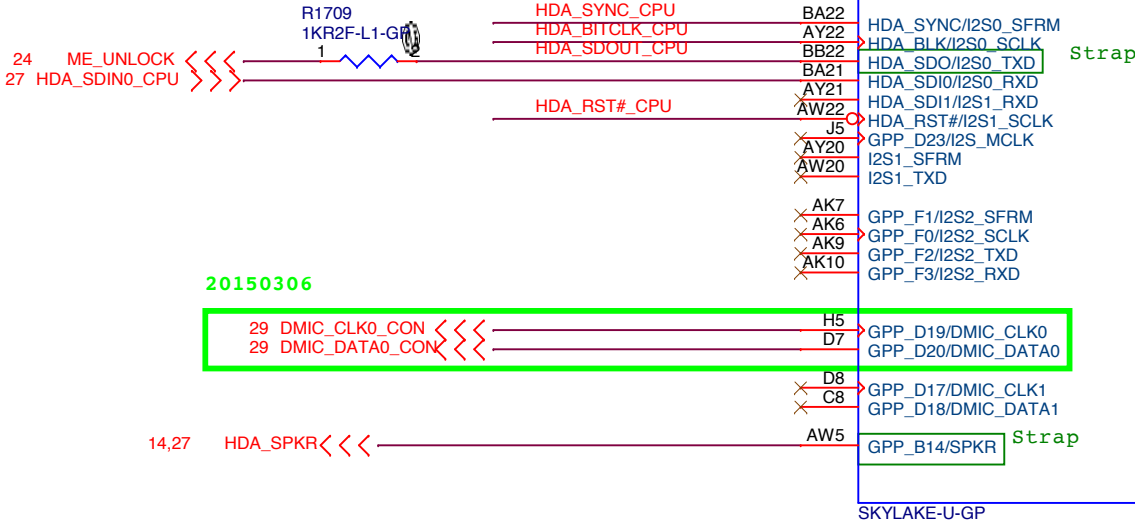
Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confidentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down



Main Func = PCH

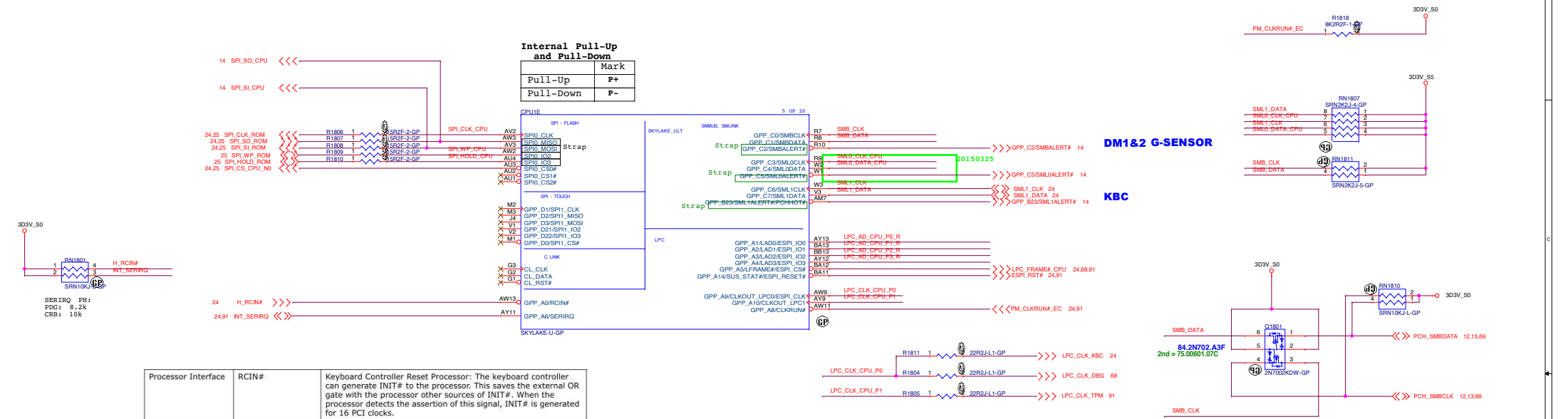


20141021 Jack



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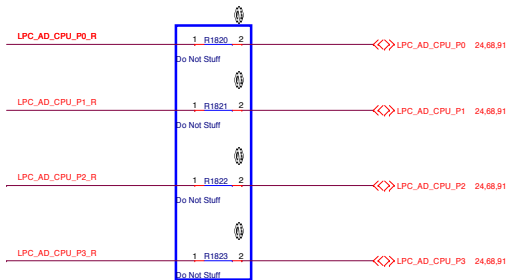
20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

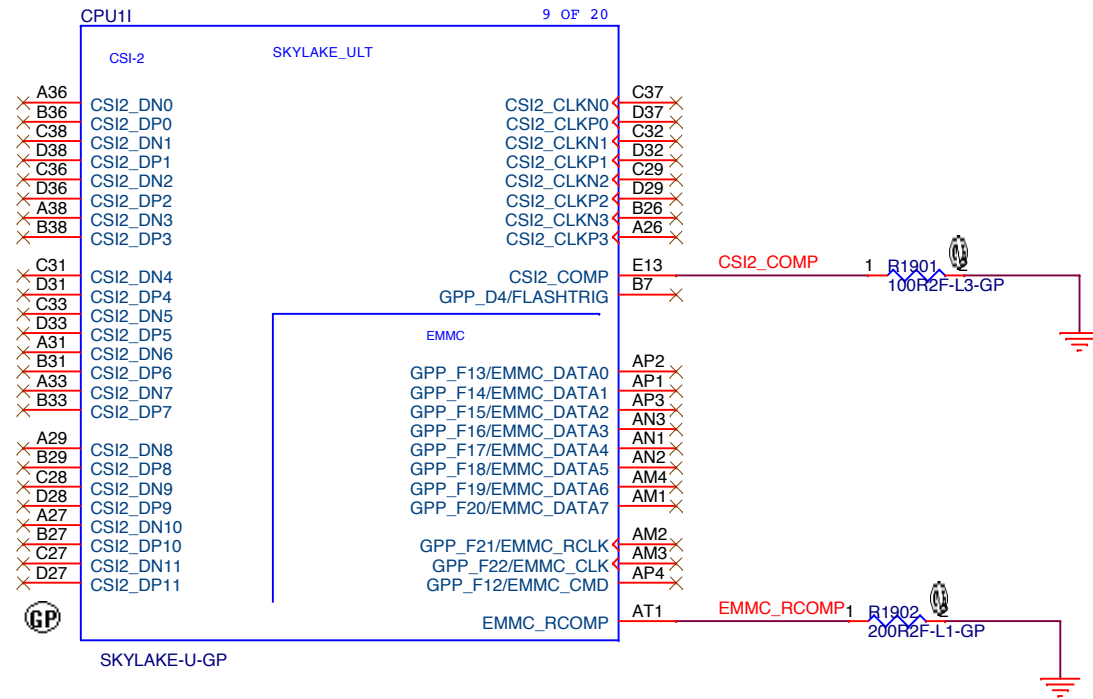
- **S – Sample Phase**, Signal driven low
- **R – Recovery Phase**, Signal driven high
- **T – Turn-around Phase**, Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.



Main Func = PCH



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Title CPU_(CS-2/EMMC)

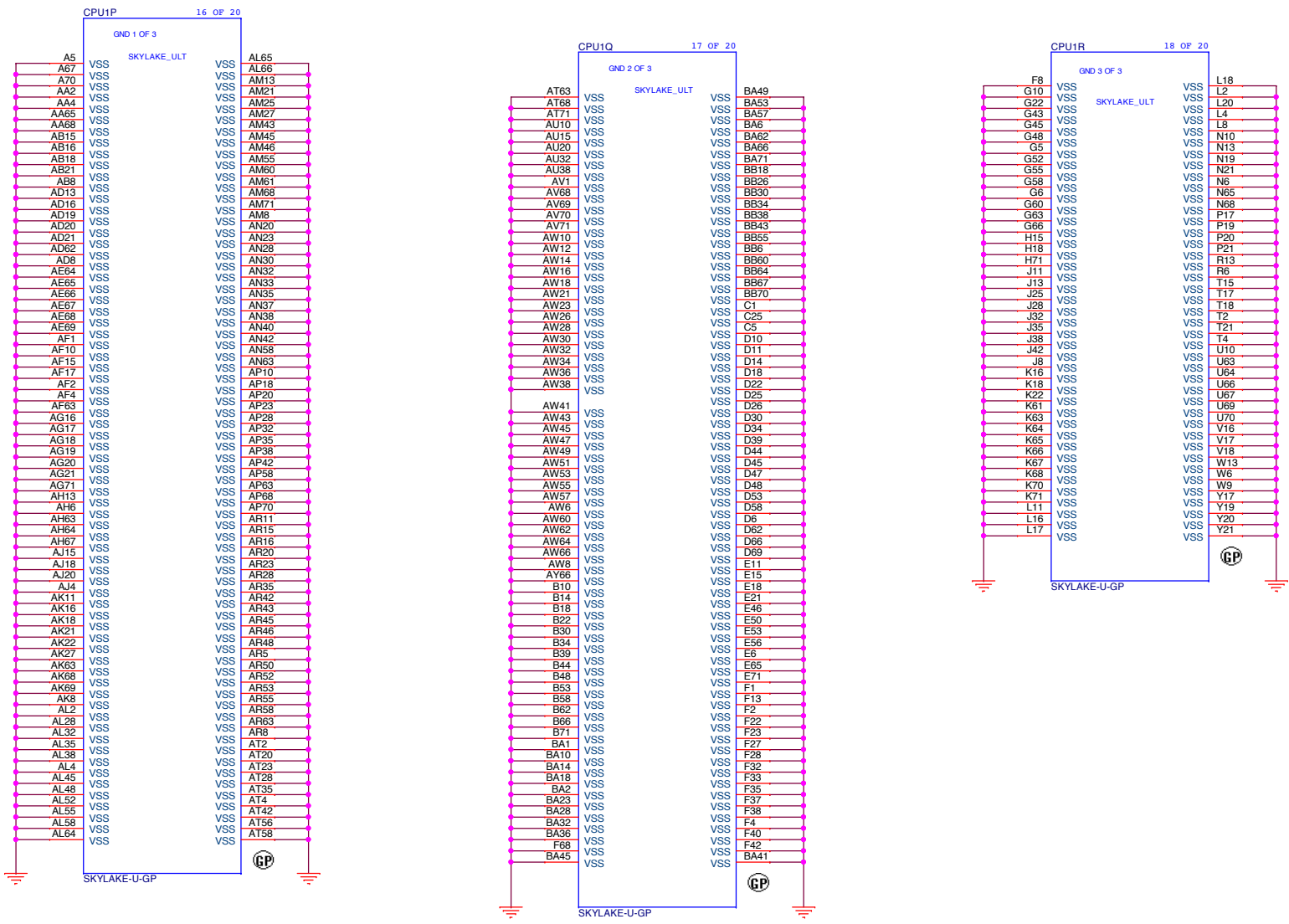
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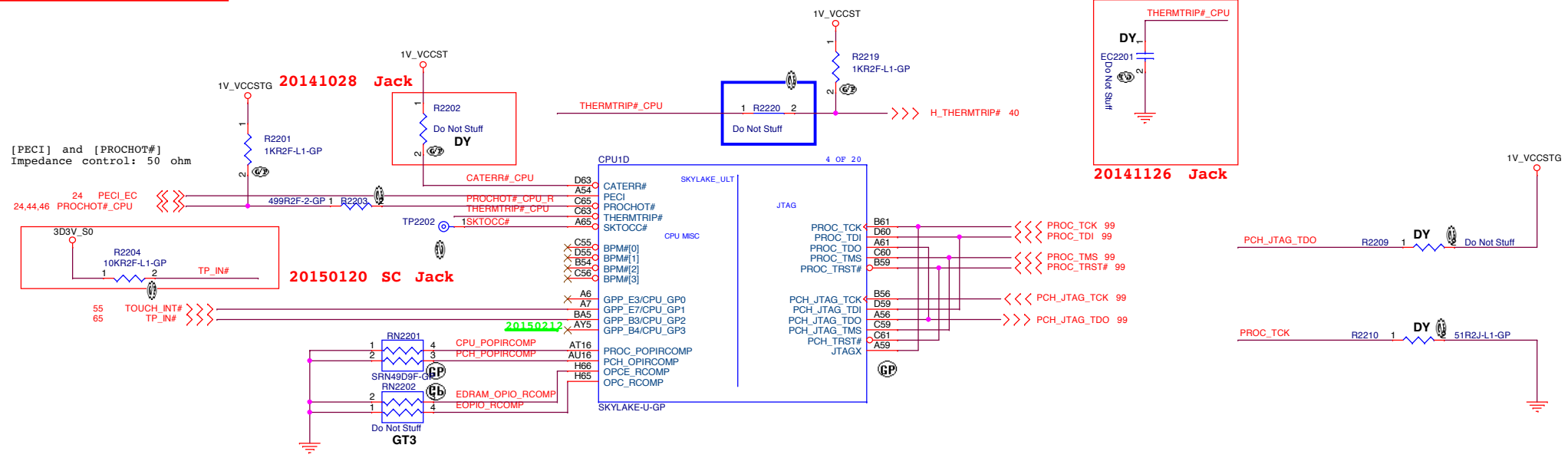
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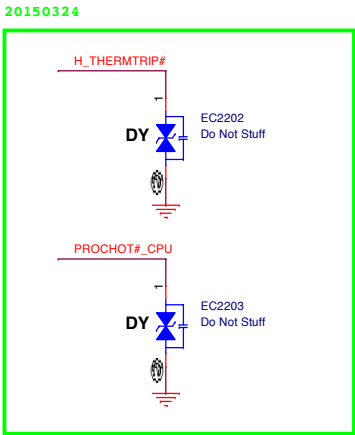
Main Func = PCH



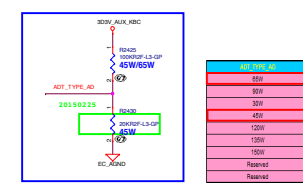
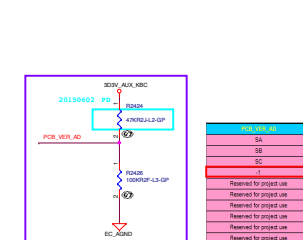
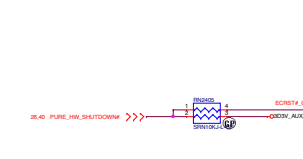
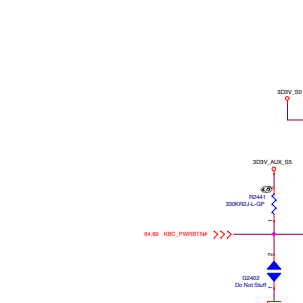
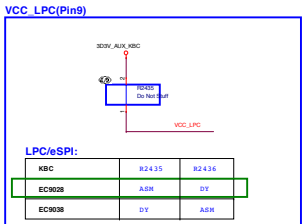
Main Func = CPU



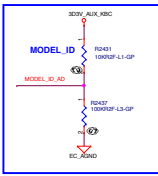
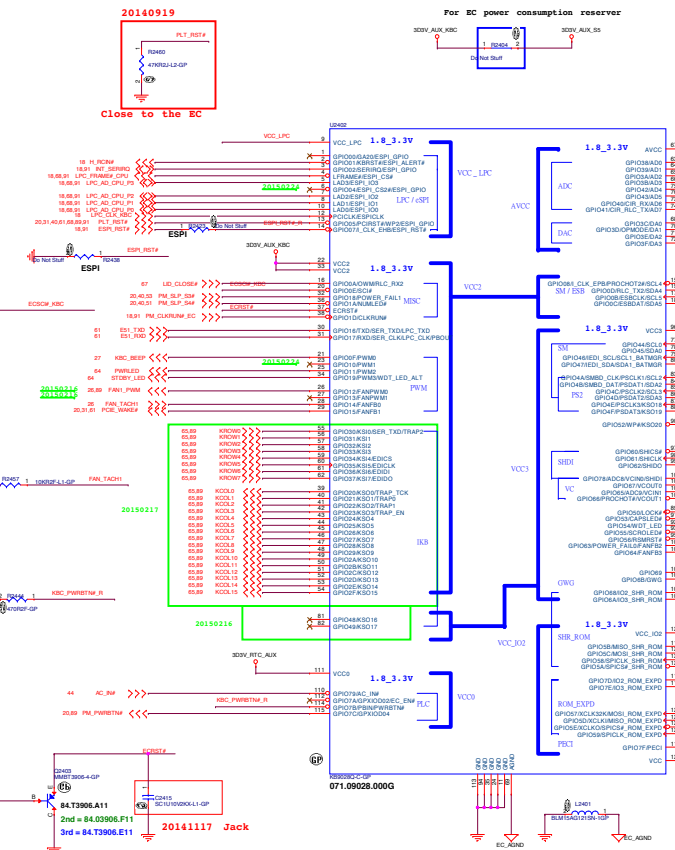
PROCHOT#	Processor Hot: PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	Thermal Trip: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines



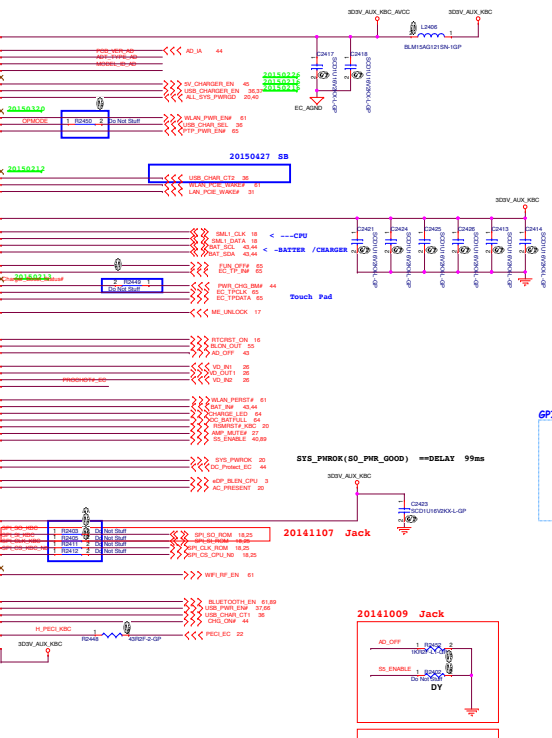
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[illegible]

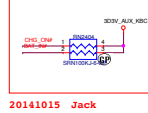
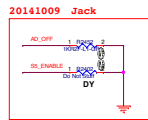
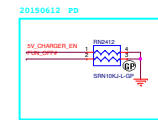
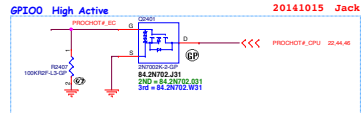
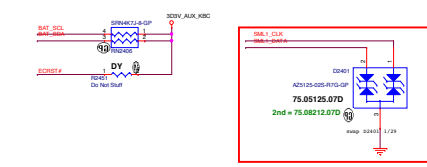
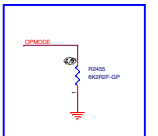
Model No.	Pull-In Voltage	Pull-Up Voltage	Rated Voltage	No. Voltage	WPC Power Rating
909	NA	102.0 V	102.0 V	1.000 V	< 0.15 W
909	100.0 V	NA	100.0 V	1.000 V	< 0.15 W
909	NA	102.0 V	102.0 V	1.000 V	< 0.15 W
456	20.5 V	105.0 V	105.0 V	0.500 V	< 0.58 W
1209	33.0 V	102.0 V	0.819 V	0.800 V	< 0.80 W
1209	47.0 V	102.0 V	1.050 V	1.075 V	< 0.87 W
1209	64.0 V	102.0 V	1.250 V	1.177 V	< 1.08 W
1209	79.5 V	102.0 V	1.400 V	1.250 V	< 1.24 W
Revised			1.600 V	1.542 V	< 1.42 W



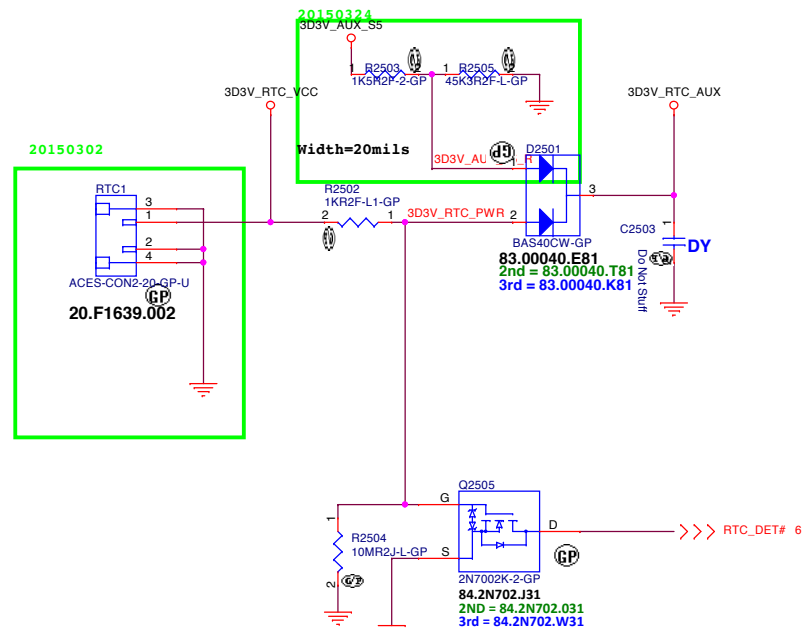
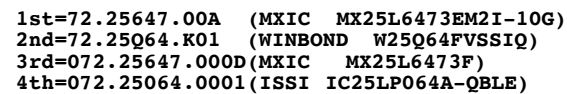
Model No./Jr	Pull-Down Regulator	Pull-Down Regulator	Typical Voltage	Max Voltage	SPC Firmware Setting
USA					
Reserved for project use	100 kΩ	10 kΩ	3.000 V	3.005 V	± 2875 V
Reserved for project use	100 kΩ	20 kΩ	2.750 V	2.750 V	± 2.616 V
Reserved for project use	100 kΩ	33 kΩ	2.481 V	2.493 V	± 2.303 V
Reserved for project use	100 kΩ	47 kΩ	2.246 V	2.259 V	± 2.065 V
Reserved for project use	100 kΩ	64 kΩ	2.051 V	2.017 V	± 1.894 V
Reserved for project use	100 kΩ	79 kΩ	1.867 V	1.843 V	± 1.708 V
Reserved for project use	100 kΩ	100 kΩ	1.693 V	1.607 V	± 1.504 V
Reserved for project use	100 kΩ	143 kΩ	1.506 V	1.374 V	± 1.281 V
Reserved for project use	100 kΩ	174 kΩ	1.269 V	1.125 V	± 1.084 V
Reserved for project use	100 kΩ	216 kΩ	1.048 V	0.972 V	± 0.861 V



EC9028	ASM (LPC)
EC9038	DY (eSPI)



Main Func = RTC



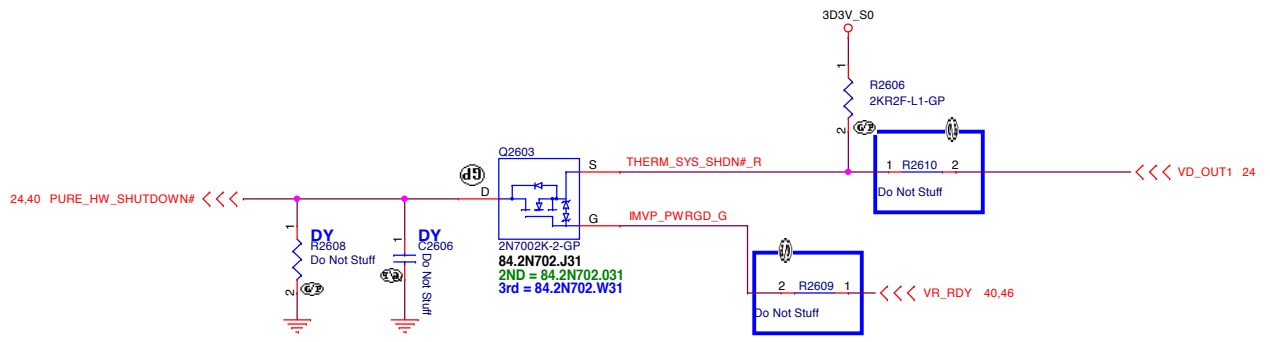
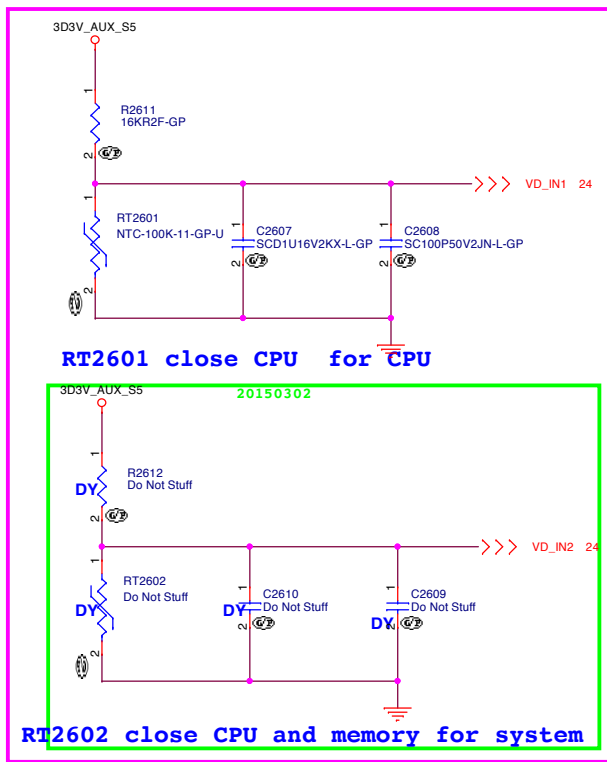
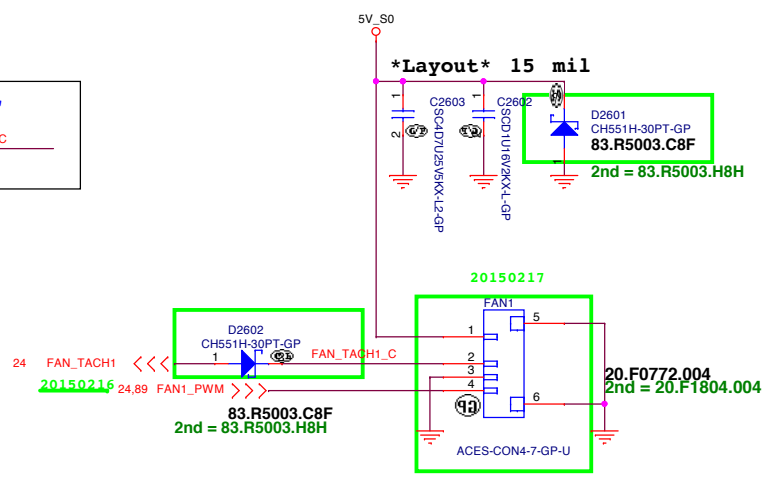
Title			
Flash(KBC+PCH)/RTC			
Size A3	Document Number		Rev
	Mihawk MB		-3
Date:	Tuesday, June 06, 2017	Sheet 25 of	105

Main Func = Thermal Sensor

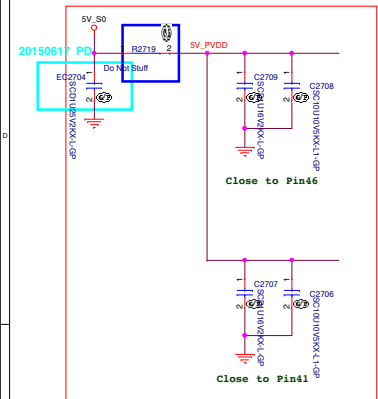
AFTP TESTPOINT

89 FAN_TACH1_C <<< FAN_TACH1_C

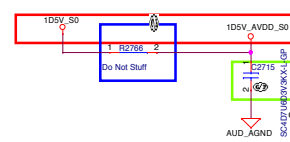
Layout 15 mil



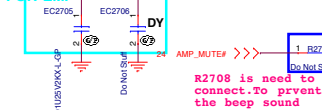
SSID = 104C



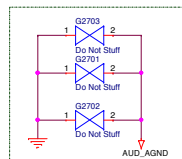
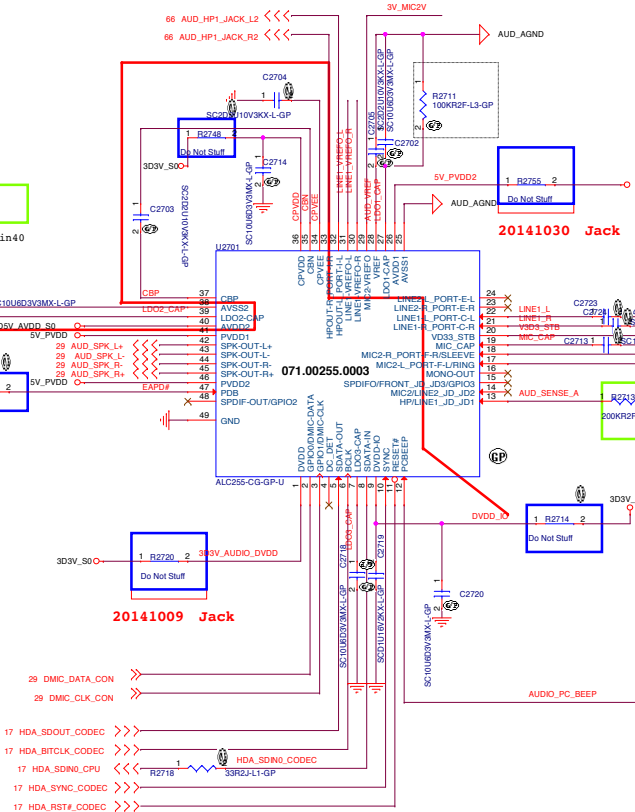
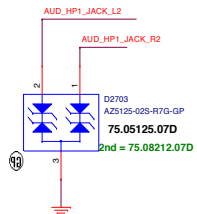
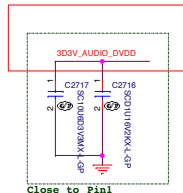
20141009 Jack



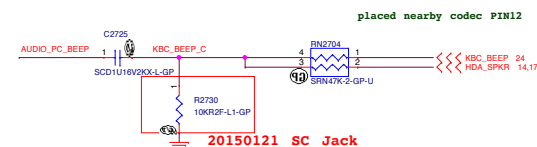
FQR



20141009 Jack



AUD_AGND close to codec 1



20150121 SC Jack

Layout Note:

Place close to Pin 26

20141030 Jack

Layout Note:

Place close to Pin 13

Layout Note:

75.05125.07D
2nd = 75.08212.07D

Width>40mil, to improve Headphone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

5

4

3

2

1

D

D

C

C

B

B

A

A

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Title		
Audio AMP 1001		
Size	Document Number	Rev
A4	Mihawk MB	-3
Date:	Tuesday, June 06, 2017	Sheet 28 of 105

5

4

3

2

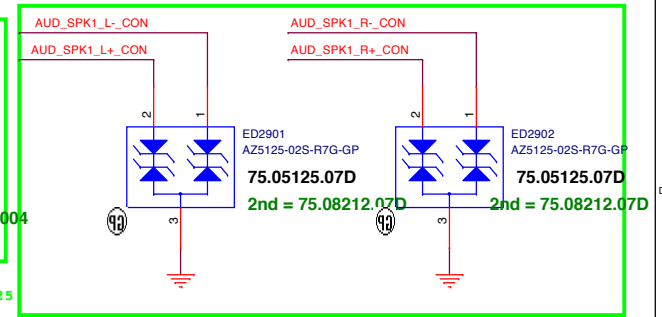
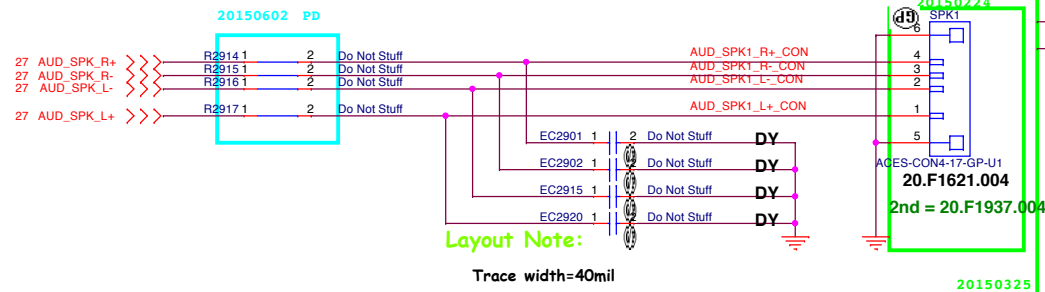
1

SSID = AUDIO

Speaker

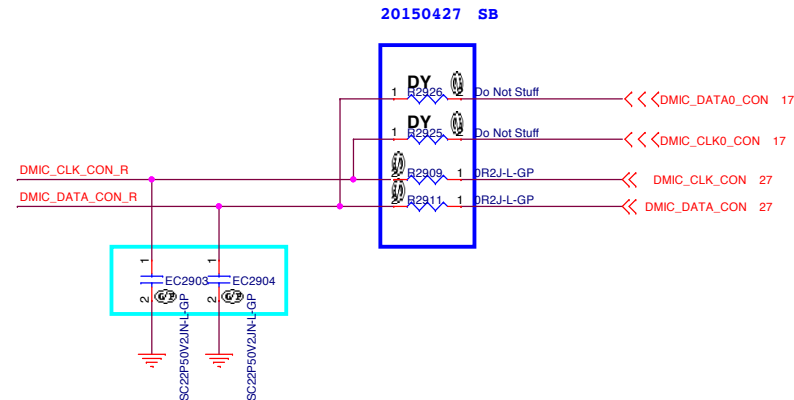
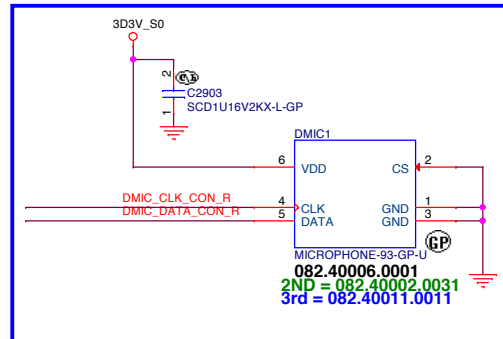
AUD_SPK1_L_-CON <<< AUD_SPK1_L_-CON 89
AUD_SPK1_L+_CON <<< AUD_SPK1_L+_CON 89
AUD_SPK1_R_-CON <<< AUD_SPK1_R_-CON 89
AUD_SPK1_R+_CON <<< AUD_SPK1_R+_CON 89

AFTP TESTPOINT



DMIC

20150427 SB



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Title

Speaker/HPMIC

Size

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A3

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Rev

-3

Date: Tuesday, June 06, 2017

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D

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C

B

B

A

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Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	321-328
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-130
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-574
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-685

Size	
A	

Document Number

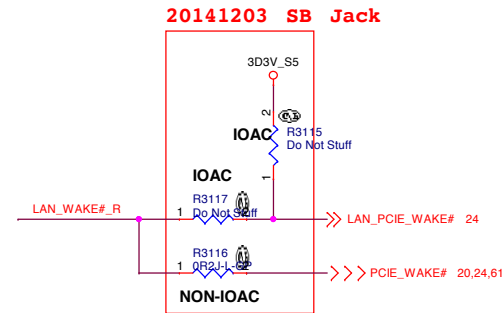
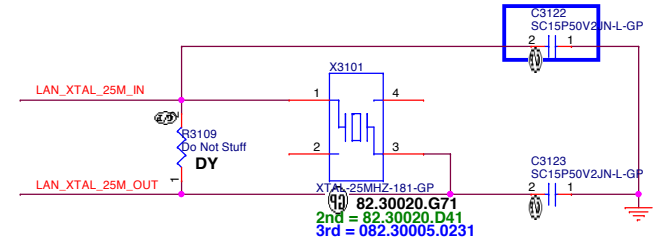
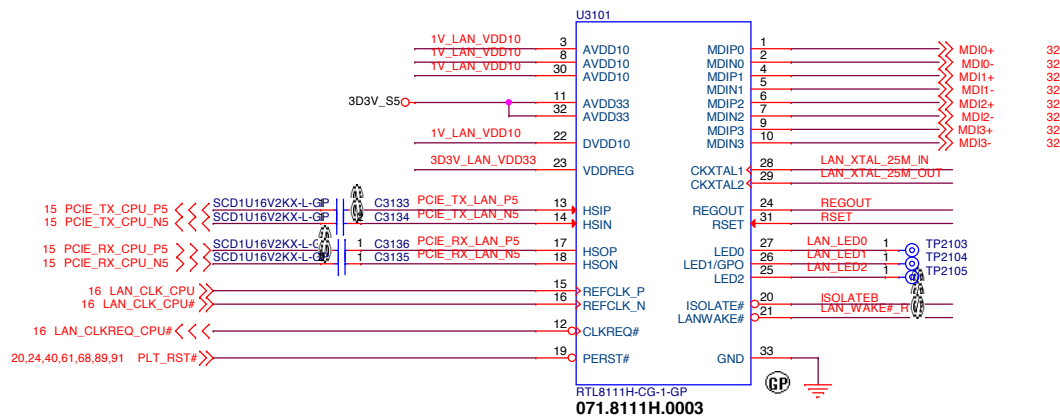
Mihawk MB

Rev

-3

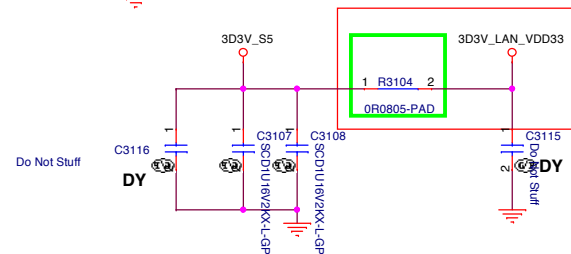
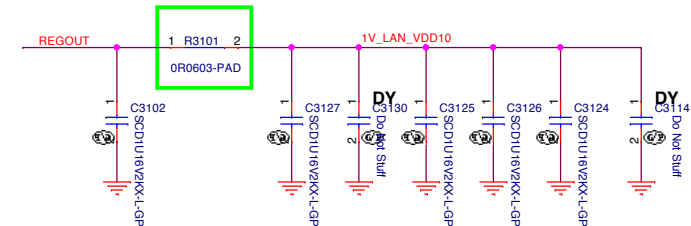
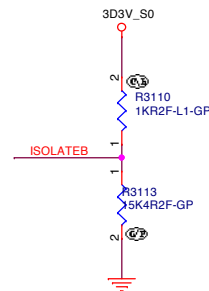
Date: Tuesday, June 06, 2017

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Layout:
For RTL8111G(S)
* Place C3121 to C3124 close to each VDD10 pin-3, 8,

C3124: close to Pin8
C3125: close to Pin30
C3126: close to Pin3
C3127: close to Pin22



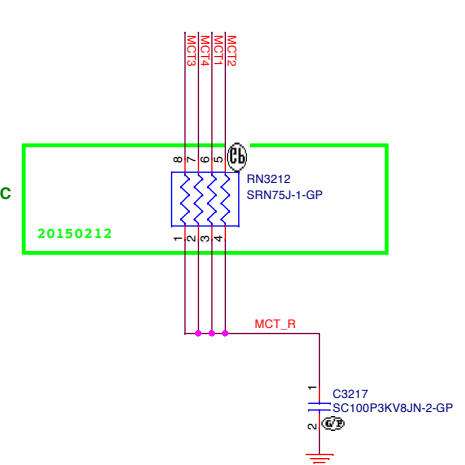
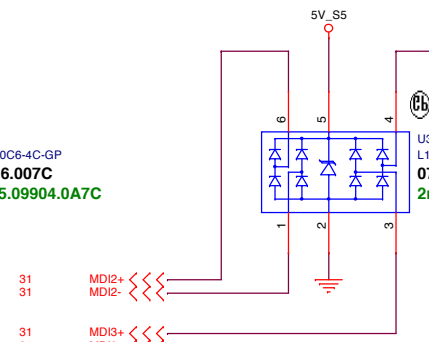
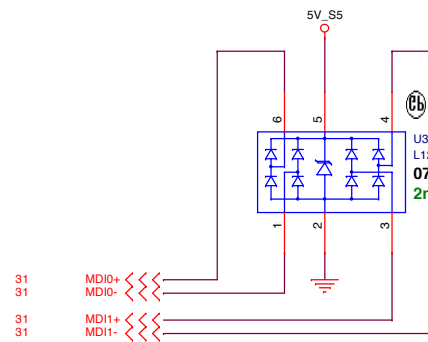
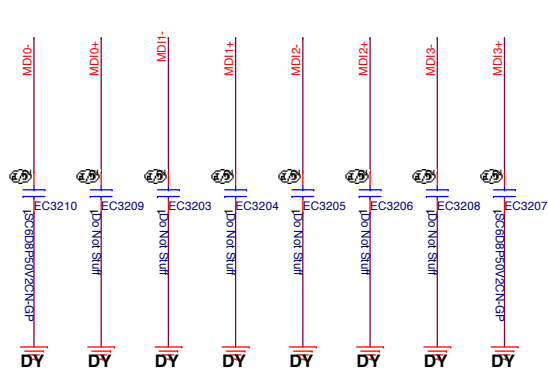
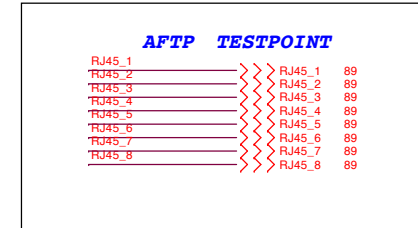
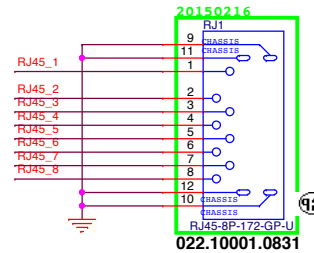
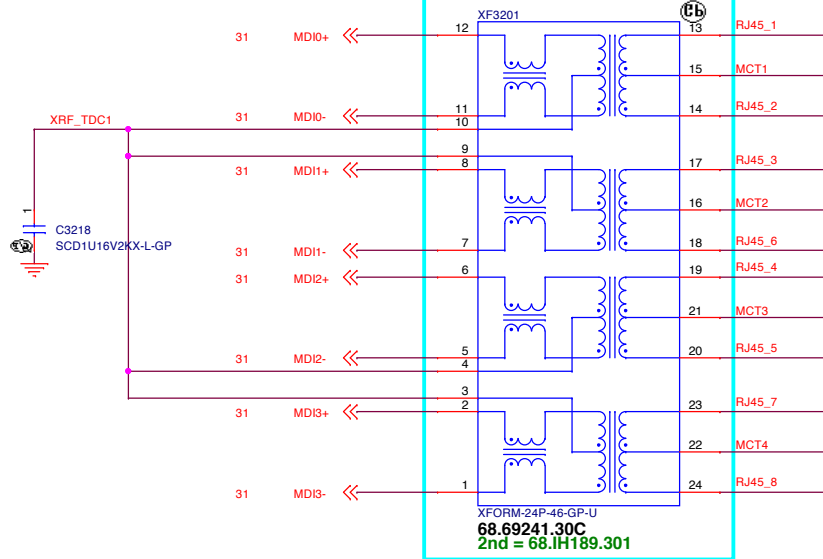
C3108.C3115: close to Pin32
C3107.C3116: close to Pin11

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Title			
LAN(RTL8111H)			
Size	Document	Number	Rev
A3	Mihawk MB		-3
Date:	Tuesday, June 06, 2017		Sheet 31 of 105

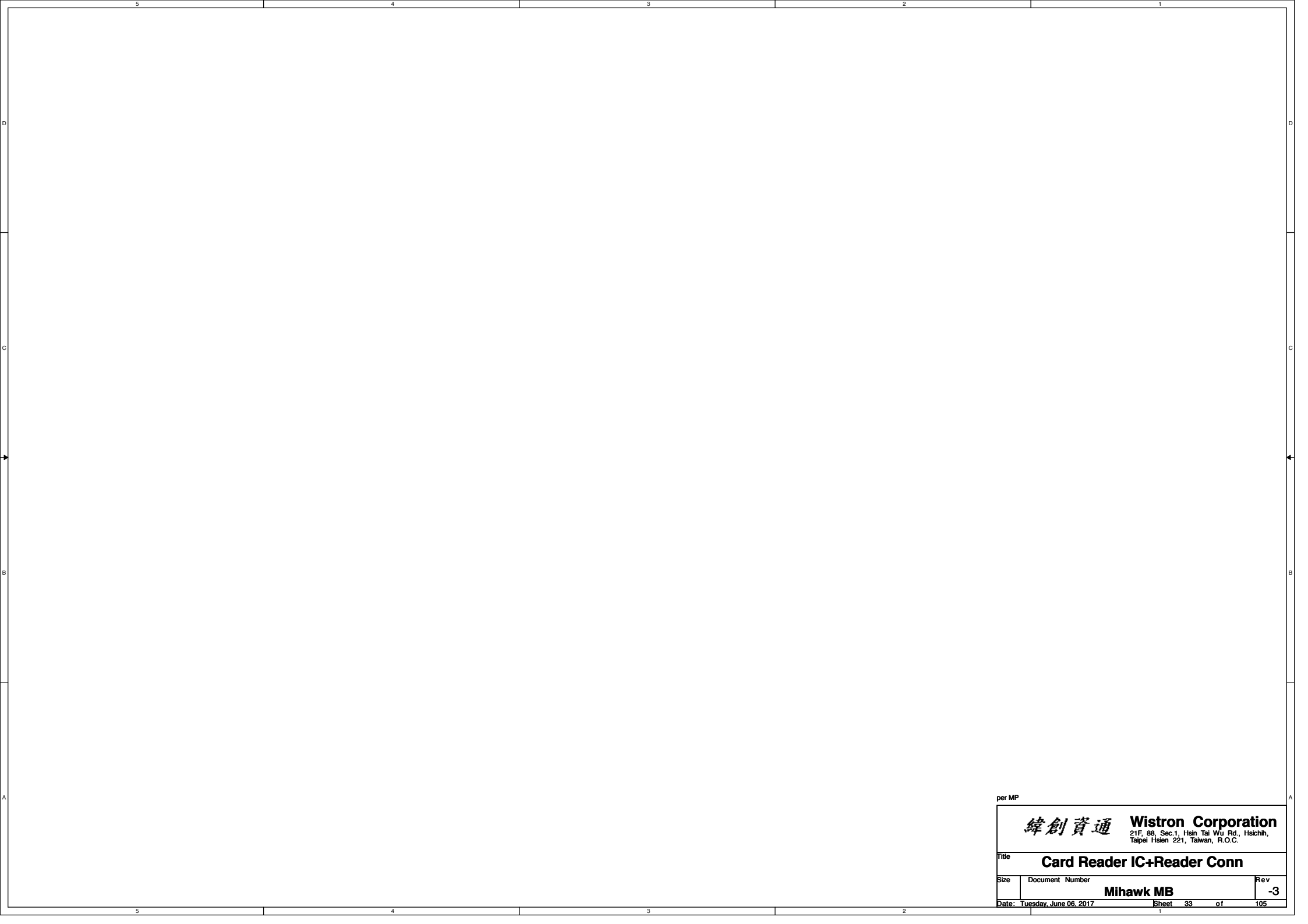
20150623 PD



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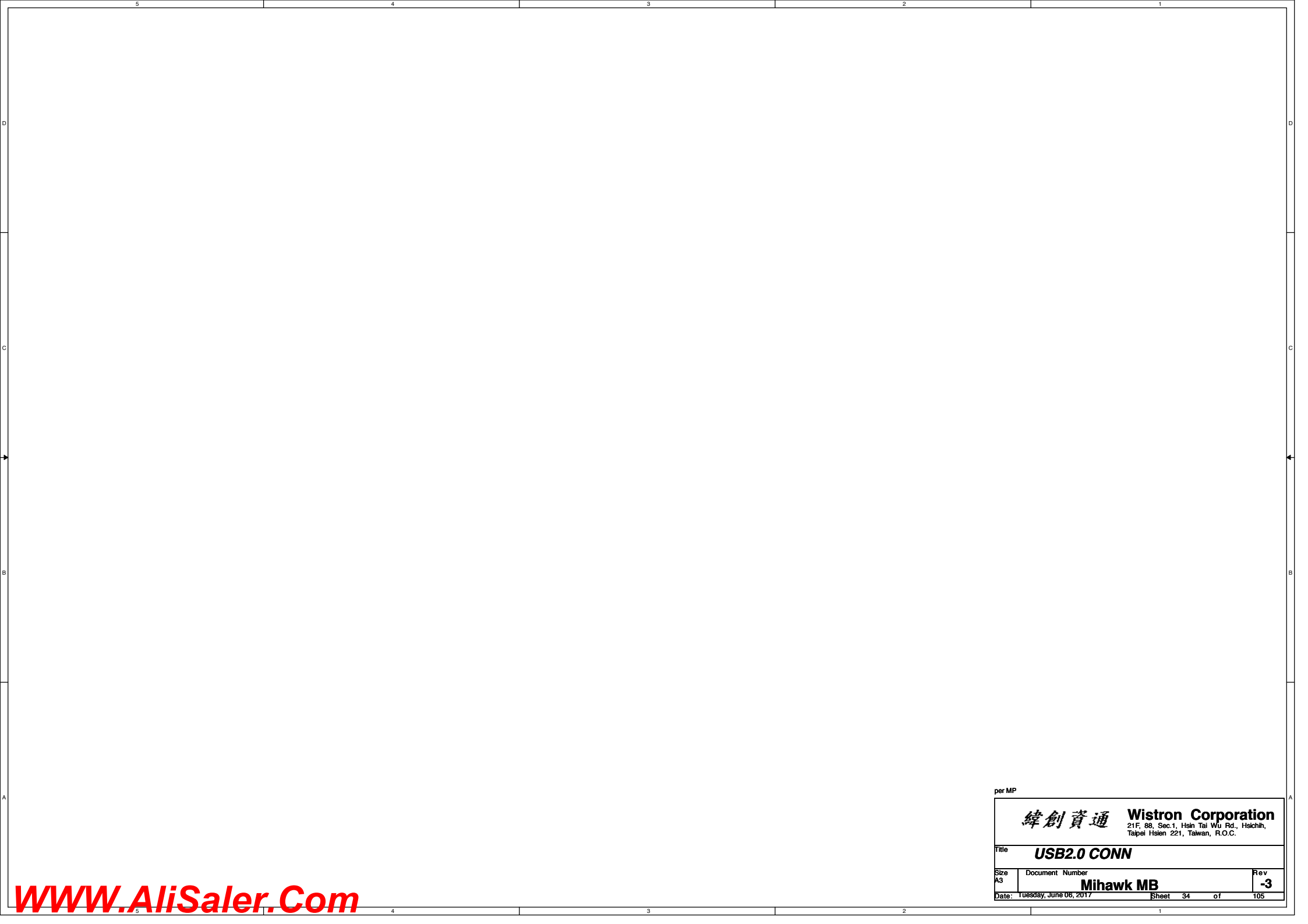
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Title			(LAN+VGA) CONNECTOR
Size	Document	Number	Rev
A3	Mihawk MB		-3
Date:	Tuesday, June 06, 2017	Sheet	32 of 105



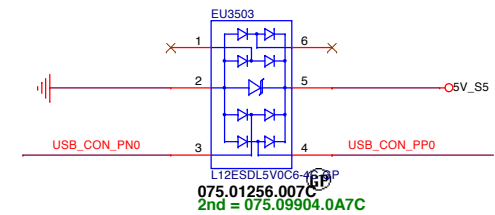
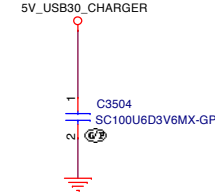
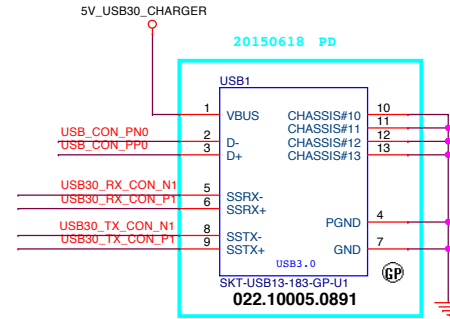
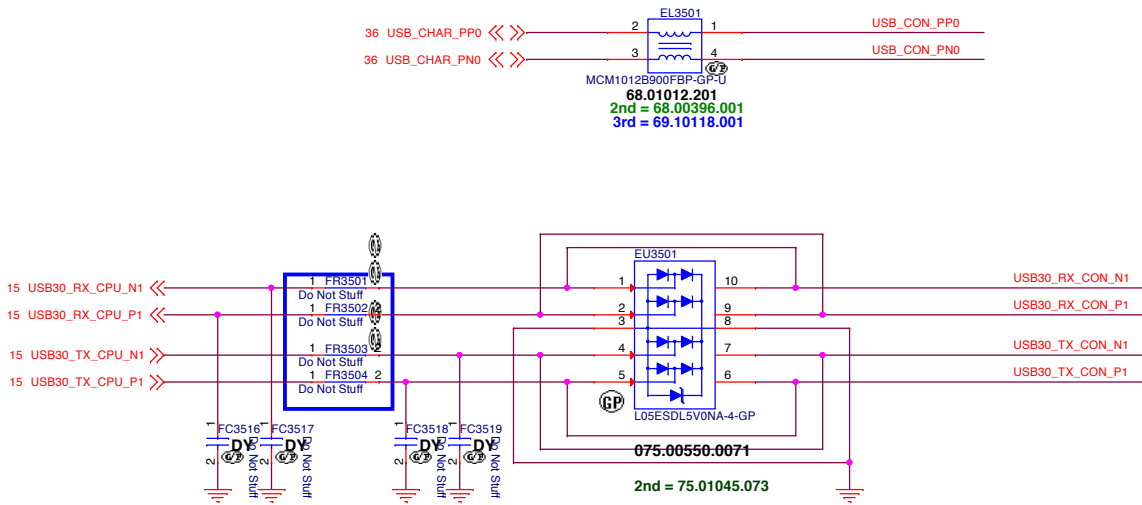
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Card Reader IC+Reader Conn			
Size	Document Number		Rev
	Mihawk MB		-3
Date:	Tuesday, June 06, 2017	Sheet 33 of	105

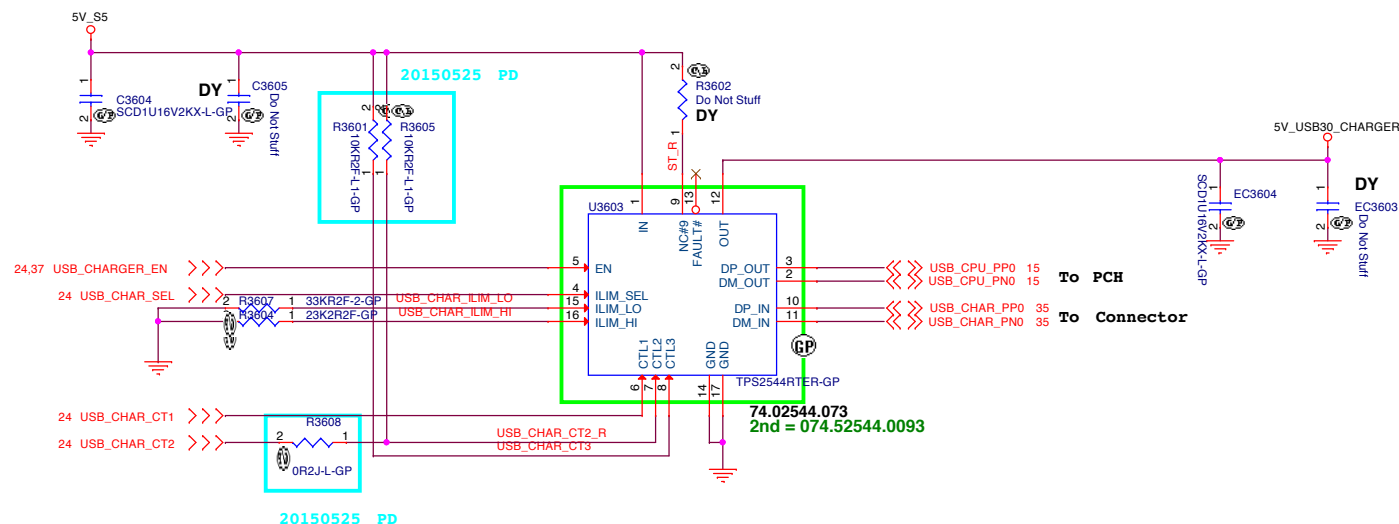


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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB2.0 CONN			
Size A3	Document Number Mihawk MB		Rev -3
Date: Tuesday, June 06, 2017		Sheet 34 of	105



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



Device Control Pins				
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	0	1	0
	0	1	1	X

3.Electrical Safety for USB3.0 Port

2.0 A <= Measurement value <= 2.2 A : Pass

1.9 A <= Measurement value < 2.0 A or 2.2 A < Measurement value <= 2.4 A : Marginal

If this result is "Marginal", 4 more samples (Total 5 samples) must be measured for each port.

And it must be confirmed that the values of 5 samples can meet our requirement (1.9 A ~ 2.4 A).

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Title

USB CHARGER

Size

Document Number

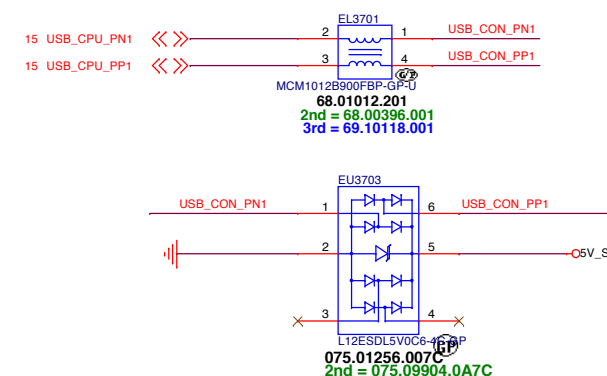
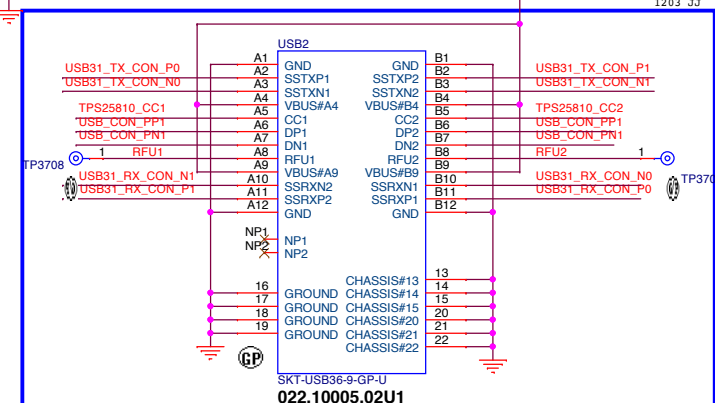
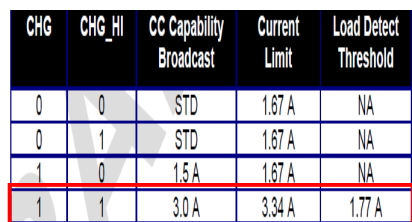
Mihawk MB

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Title

USB Redriver

Size
A3

Document Number
Mihawk MB

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Date: Tuesday, June 06, 2017

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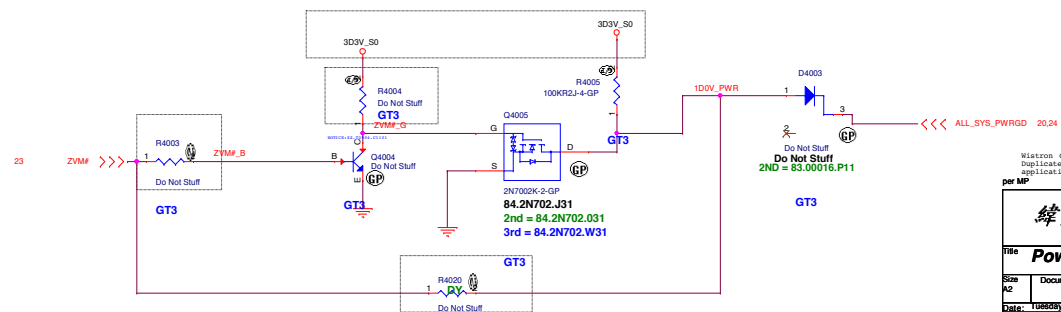
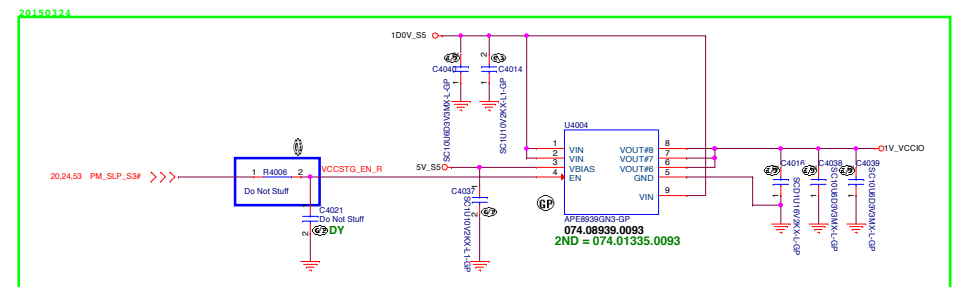
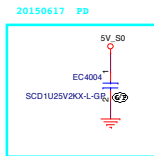
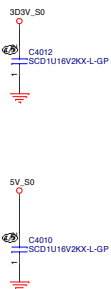
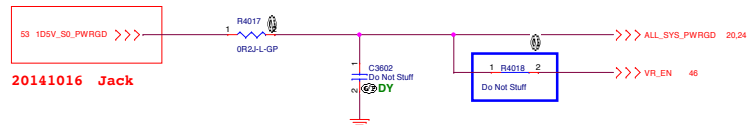
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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Title			
Size Custom	Document	Number	Rev
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Mihawk MB		-3	

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Size A2	Document Number Mihawk MB	Rev -3
Date: Tuesday, June 08, 2017	Sheet 40 of 105	

5	4	3	2	1
D				
C				
B				
A				

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Title

DS3

Size

A4

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Title

DCIN JACK

Size

A3

Document Number

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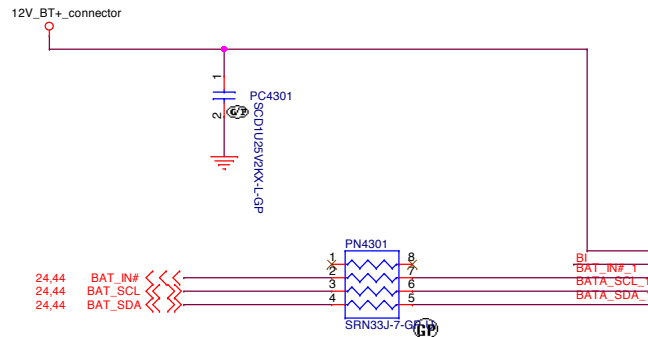
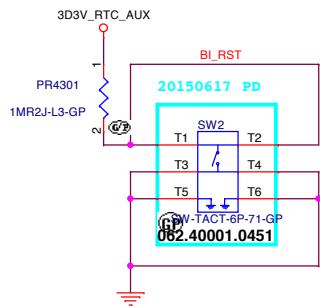
Date: Tuesday, June 06, 2017

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Rev

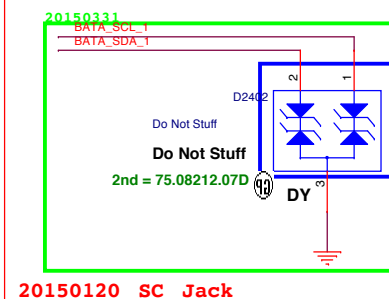
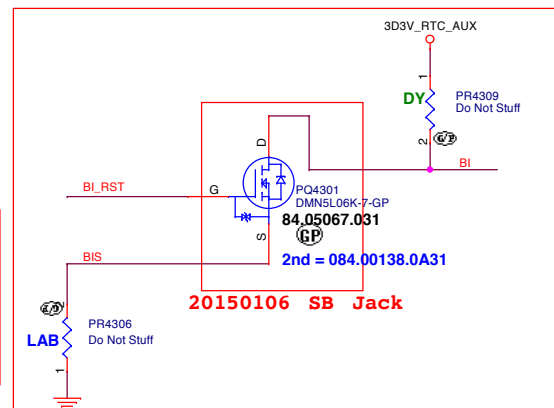
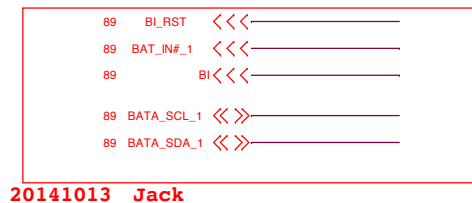
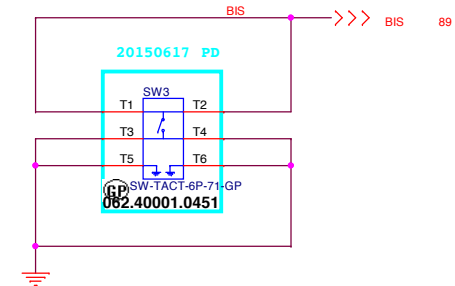
-3

Battery Reset



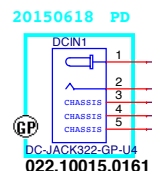
Battery Connector

Battery Insert



ANNIE solution

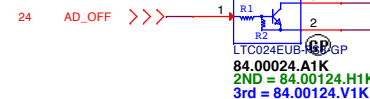
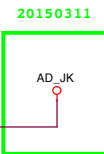
Adaptor in to generate DCBATOUT



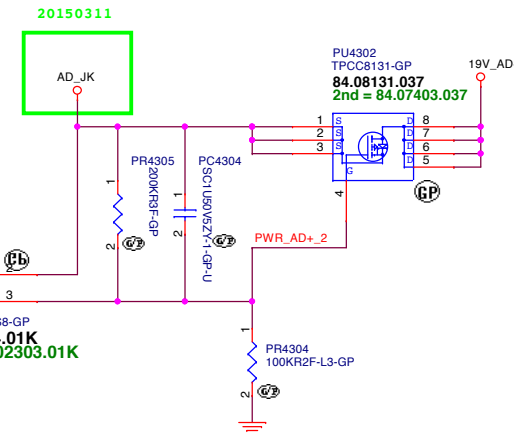
DC-JACK322-GP-UP
022.10015.0161

PD4310
P6SMBJ20A-GP
83.P6SMB.AAG
2nd = 083.00020.00AG

20150311



84.00024.01K
2ND = 84.02303.01K

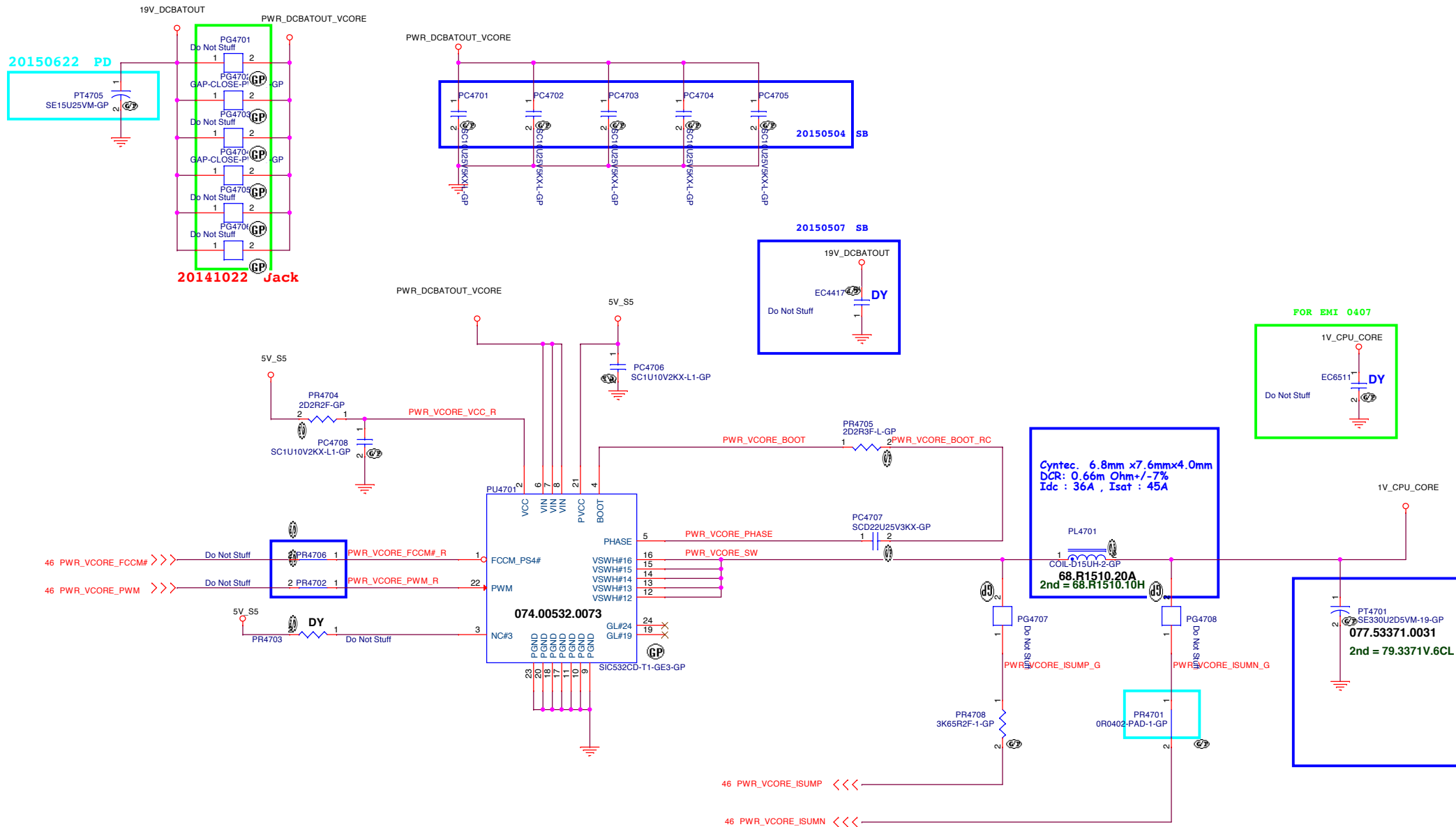


per MP

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per MP		 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
緯創資通			
Item CPU_VCORE(1/3)			
Size A2	Document Number	Mihawk MB	
Date: 1/6/2009, JUN 05, 2017	Sheet 46 of 105	Rev -3	

Main Func = CPU_CORE



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Taipei Hsien 221, Taiwan, R.O.C.

Title

VCCGTUS

Size

A2

Document Number

Mihawk MB

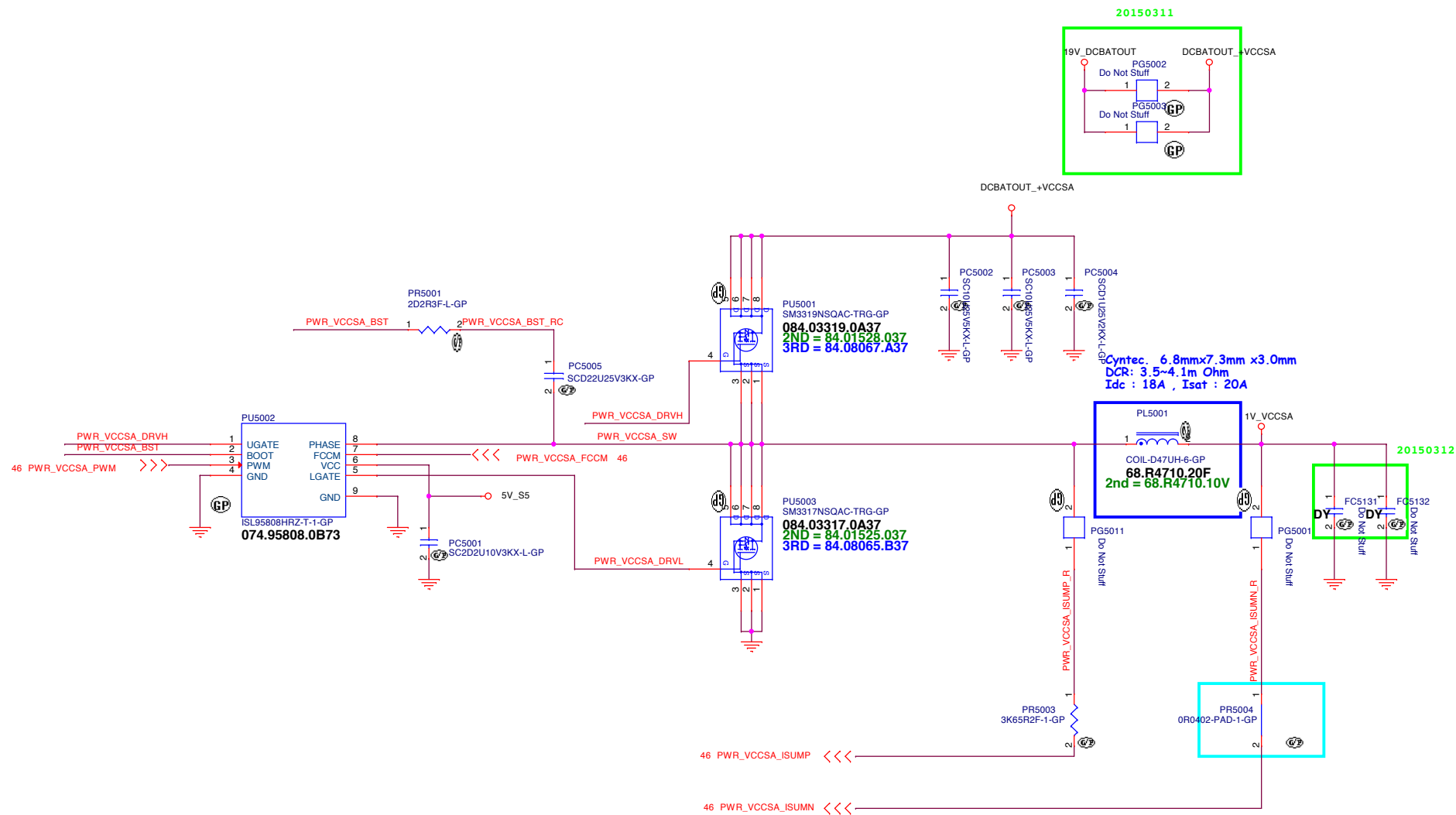
Rev

-3

Date: Tuesday, June 06, 2017

Sheet 49 of 106

Main Func = CPU_CORE



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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	VCCSA
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Size	Document Number
A3	11-1111-1111

Minhawk
Date: Tuesday, June 06, 2017

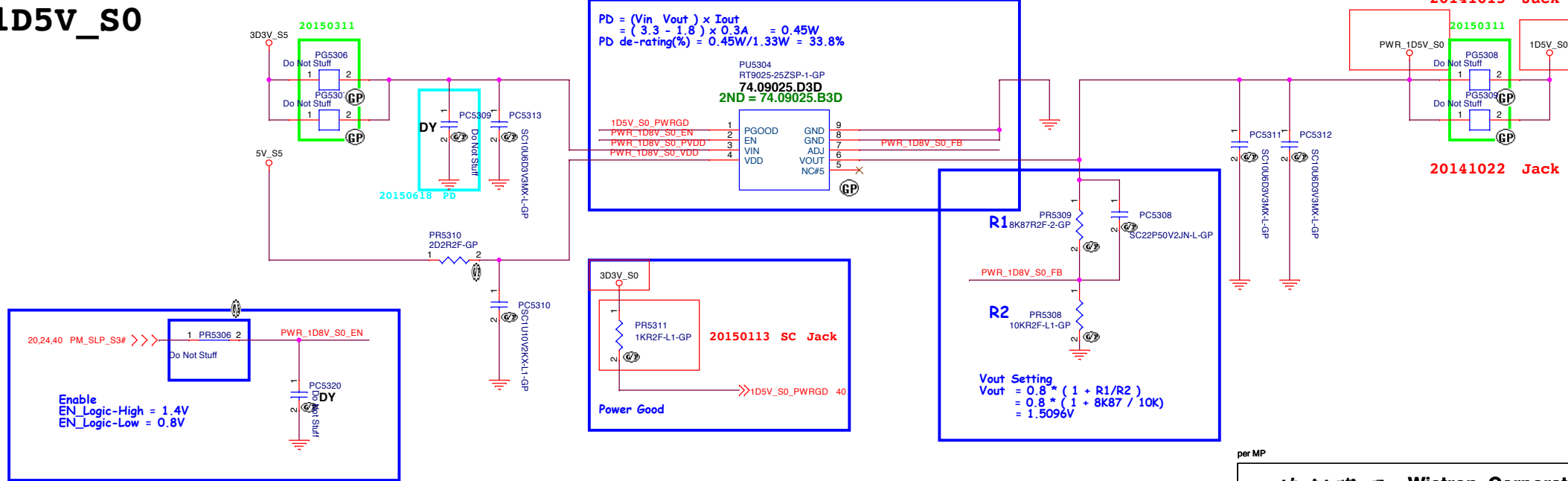
Sheet 50 of 105

Rev	2
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105



1D5V_S0



緯創資通

Title **RT8068_1D8V**

A3	Mihawk MB
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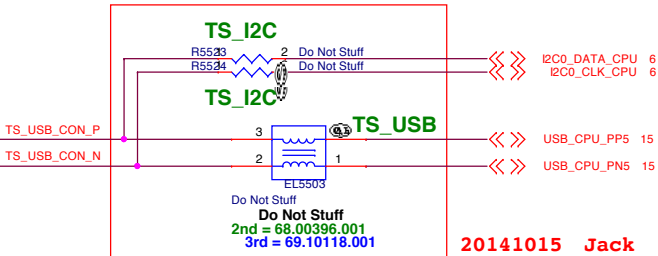
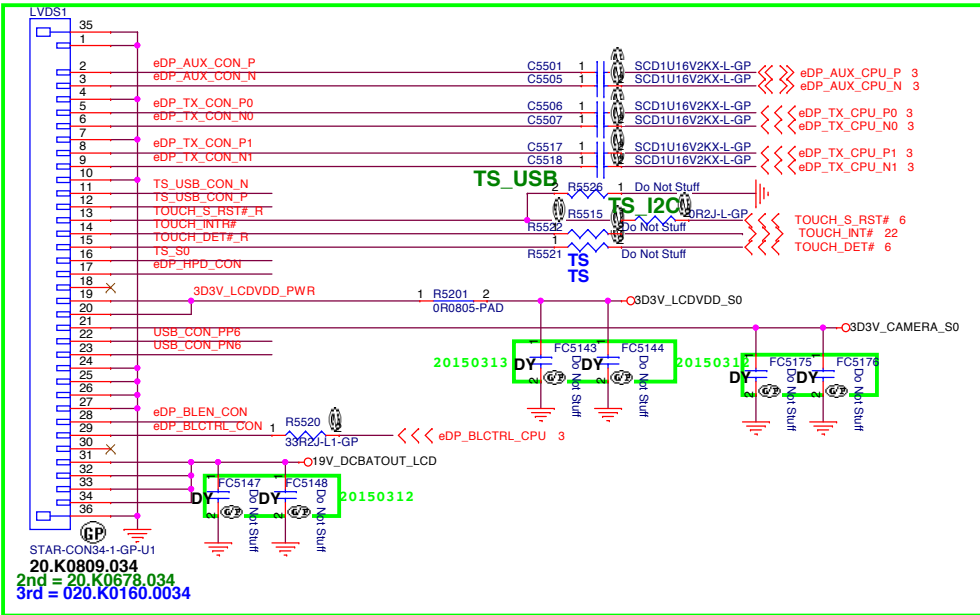
Sheet 53 of 105

Rev
-3

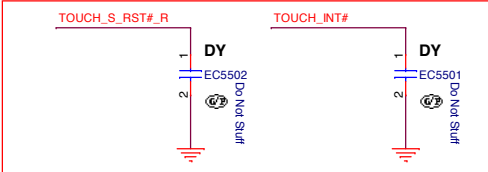
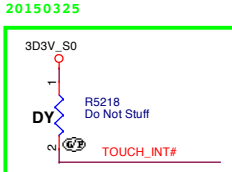
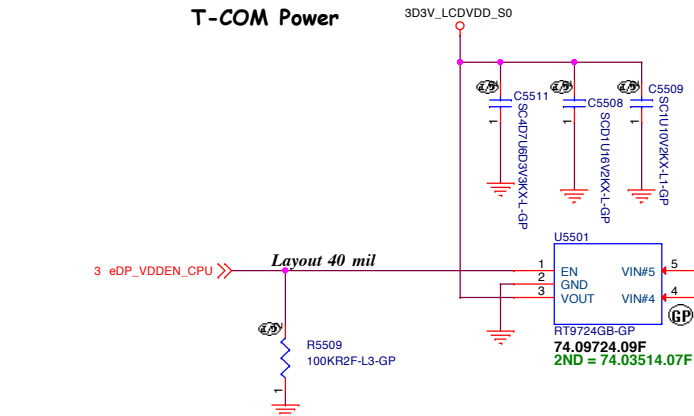
per MP

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Mihawk MB</div>	Rev <div>-3</div>
Date: Tuesday, June 06, 2017		Sheet 54 of 105

Main Func = LCD

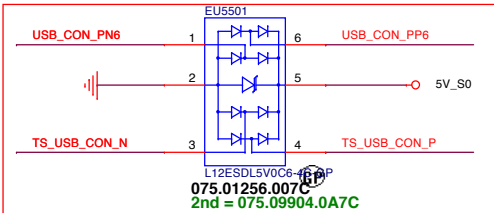
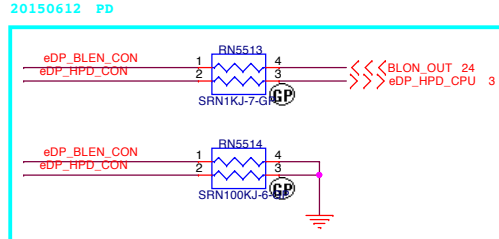
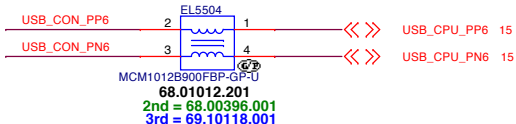
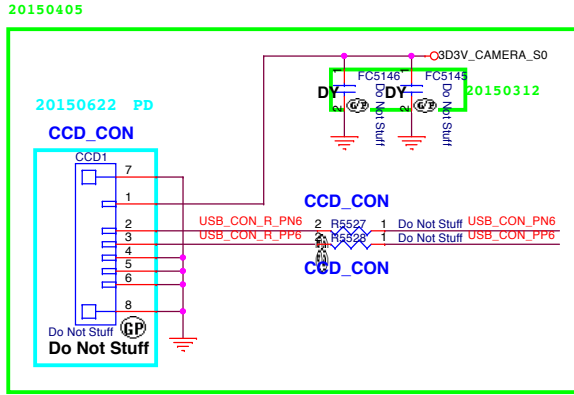
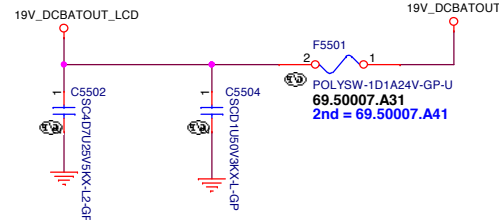


T-COM Power



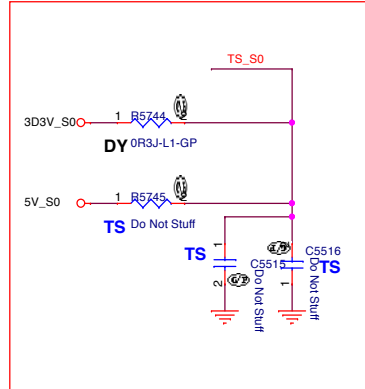
20141016 Jack

Inverter Power

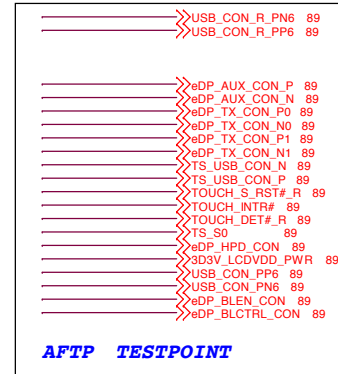


20141016 Jack

Touch panel Power



20141015 Jack

**AFTP TESTPOINT**

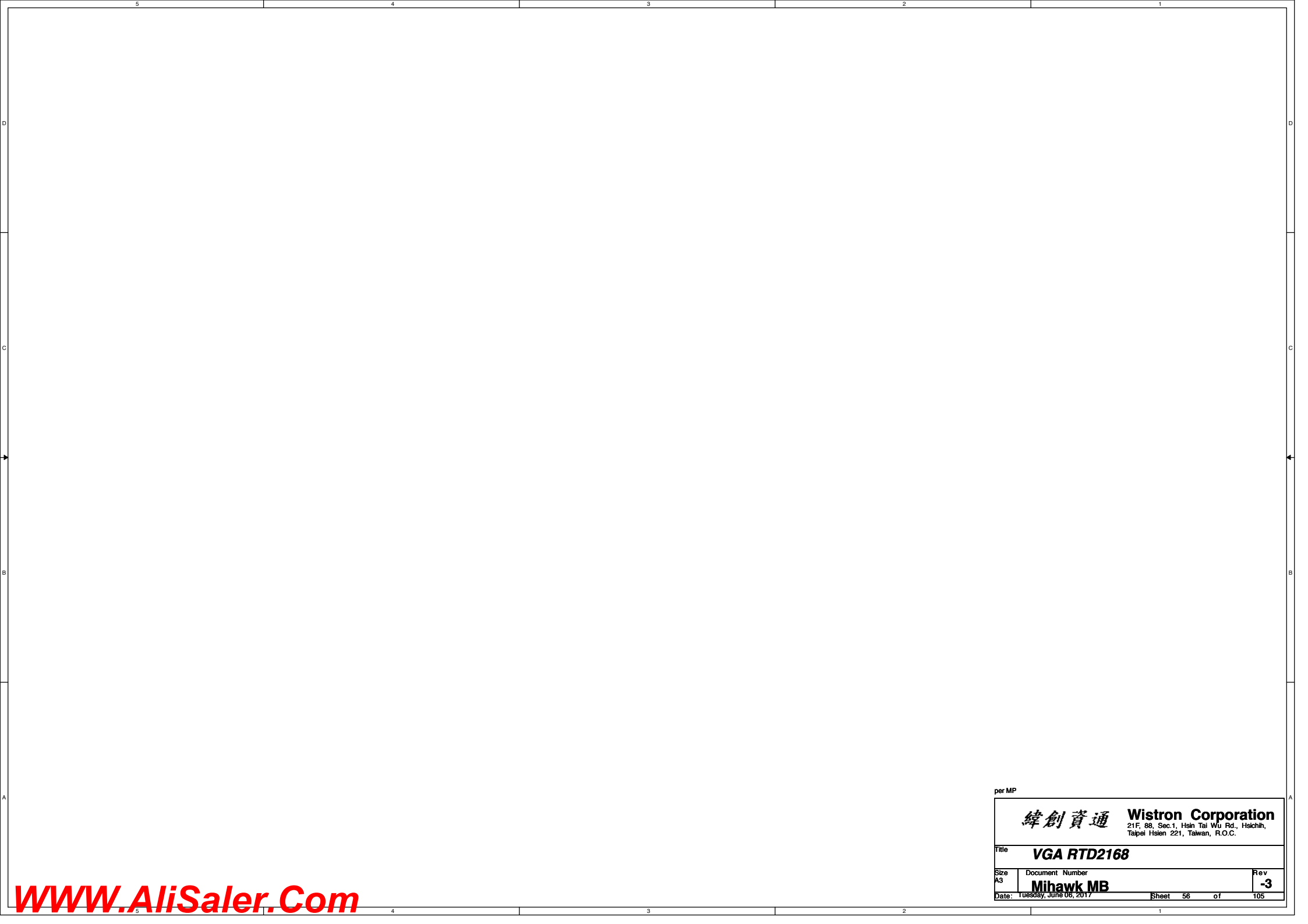
per MP

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD CONN
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Size A3	Document Number Mihawk MB
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Rev
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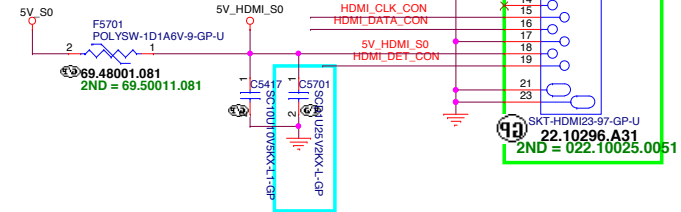
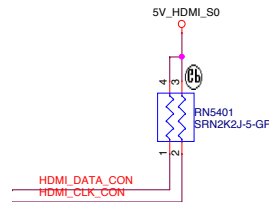
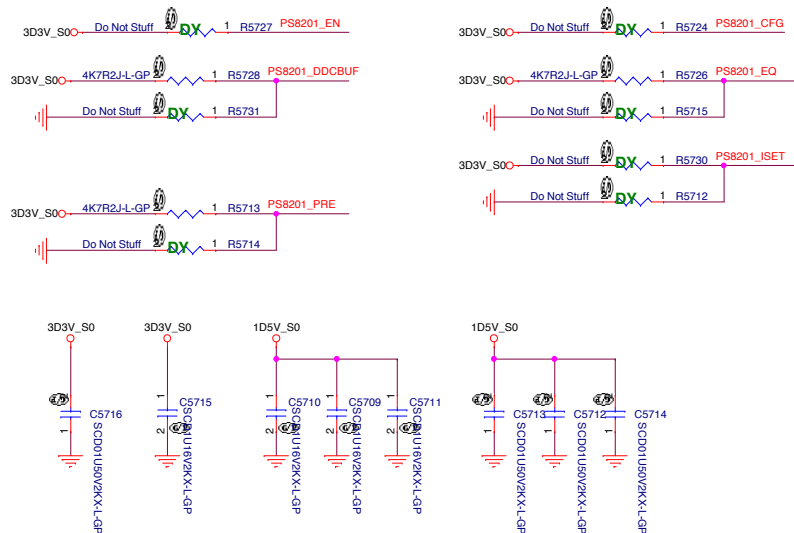


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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title VGA RTD2168			
Size A3	Document Number Mihawk MB		Rev -3
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SSID = VIDEO

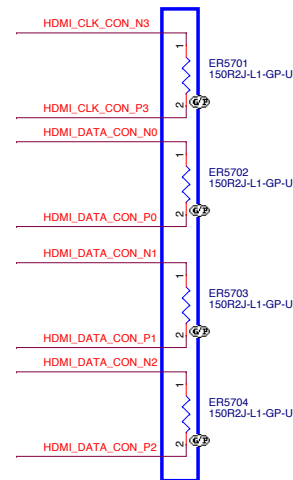
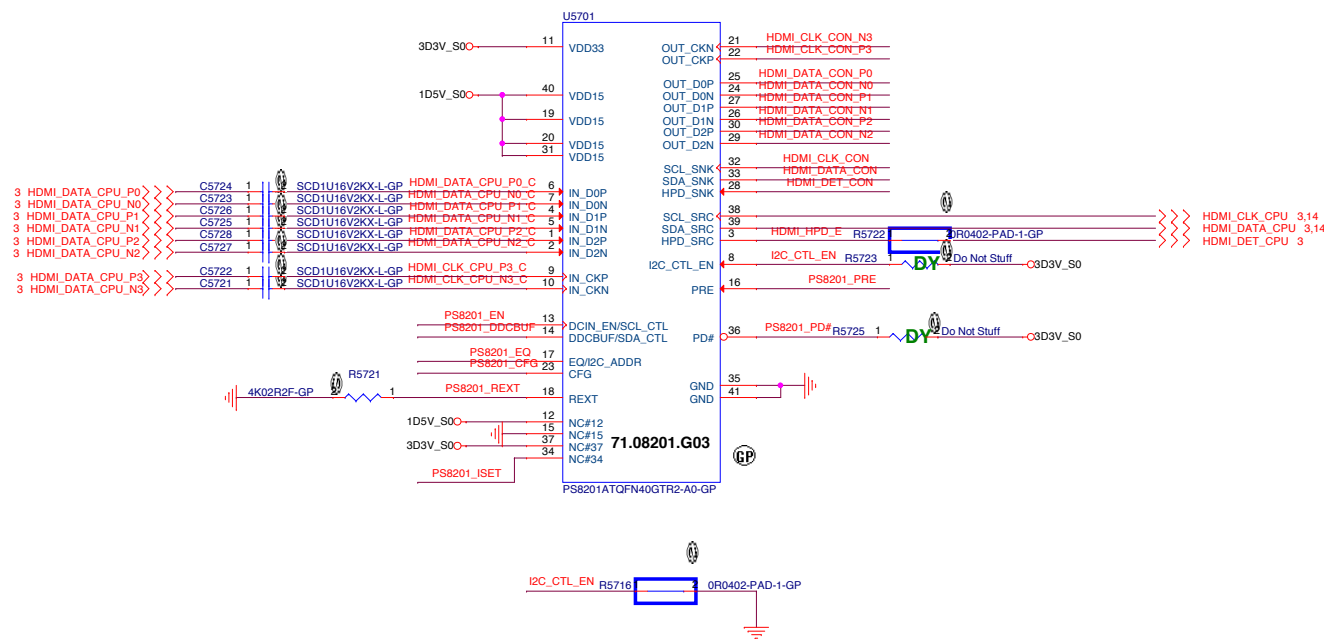
HDMI Level Shifter & CONNECTOR



HDMI CONN

20150216

20150507 SB



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Title			
HDMI Level Shifter/Conn			
Size	Document Number	Rev	
Custom	Mihawk MB	-3	
Date:	Tuesday, June 06, 2017	Sheet	57 of 105

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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	321-328
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-130
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-574
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	890-897

Size

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Document Number

Mihawk MB

Rev

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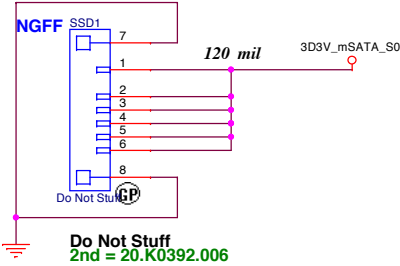
Date: Tuesday, June 06, 2017

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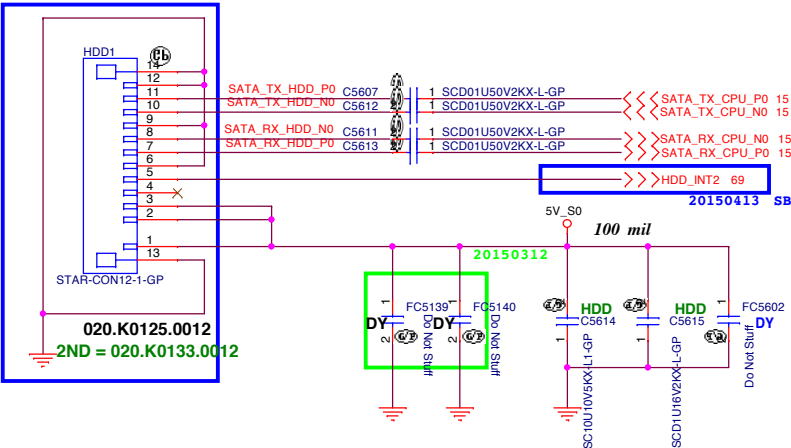
	5	4	3	2	1
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C					C
B					B
A				<div>per MP</div> <div> <div> <div>緯創資通</div> <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div> <div> <div>Title</div> <div>DVI</div> <div> <div>Size A</div> <div>Document Number</div> <div>Rev</div> </div> <div> <div>Mihawk MB</div> <div>-3</div> </div> </div> <div> <div>Date: Tuesday, June 06, 2017</div> <div>Sheet 59 of 105</div> </div> </div>	A
	5	4	3	2	1

SATA HDD / SSD Connector

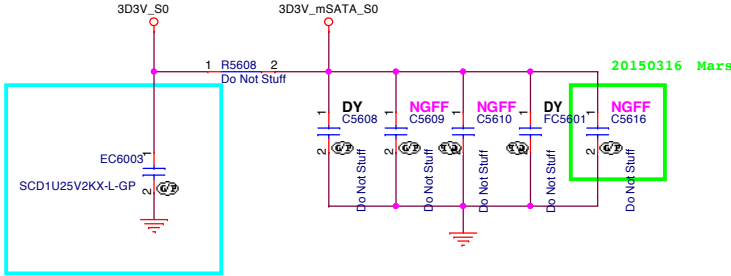
20150216



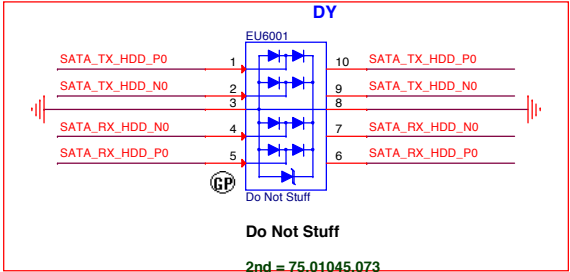
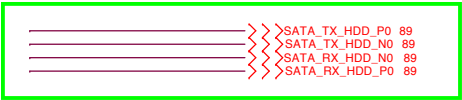
20150427 SB



AC coupling caps near connector < 100 mils
Delay HDD power off timing for 800ms-900ms after SATA controller shut down.



20150316 Mars



20150305 SC Jack

per MP

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Taipei Hsien 221, Taiwan, R.O.C.

Title HDD / NGFF SSD

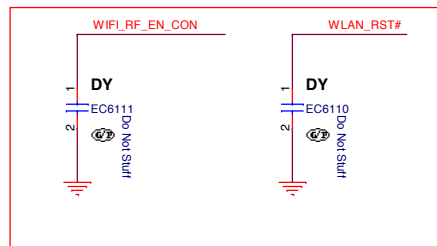
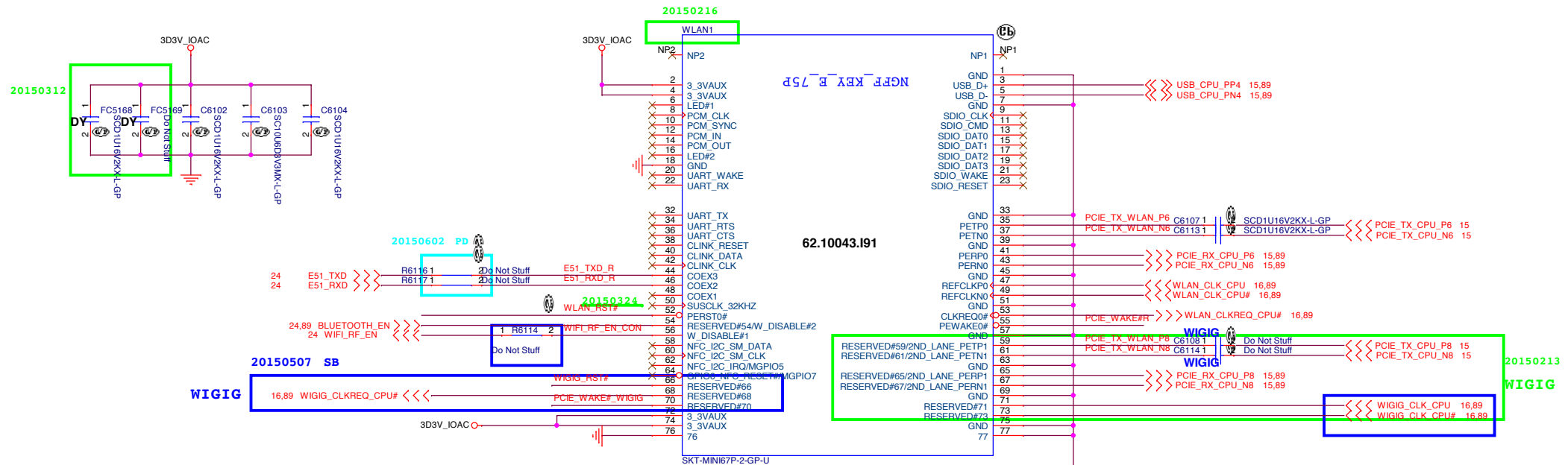
Size A3 Document Number Mihawk MB

Date: Tuesday, June 06, 2017

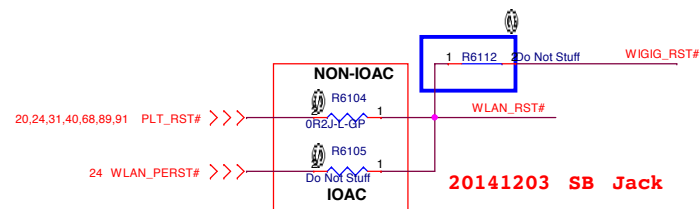
Sheet 60 of 105

Rev -3

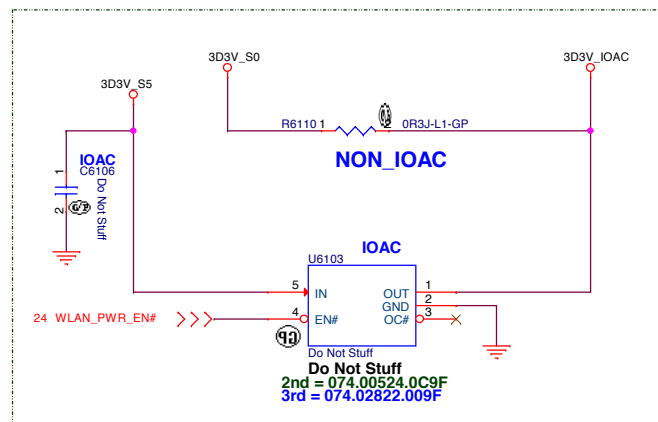
SSID = Wireless *Mini Card Connector(802.11a/b/g/n)*



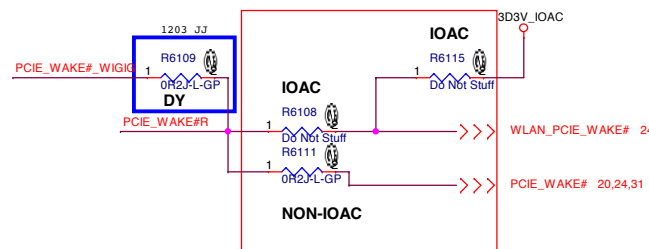
20141016 Jack



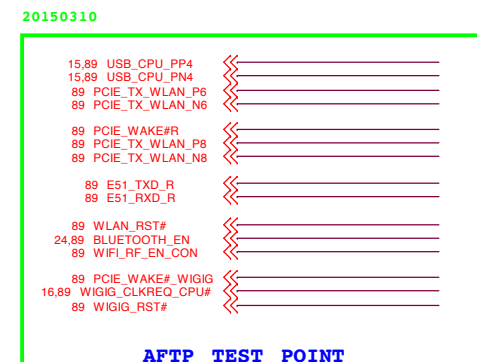
20141203 SB Jack



Do Not Stuff
2nd = 074.00524.0C9F
3rd = 074.02822.009F



20141203 SB Jack



AFTP TEST POINT

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Title	Mini Card-WLAN
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Size A3	Document Number Mihawk
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Rev
-3

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Title

Wireless Charging

Size

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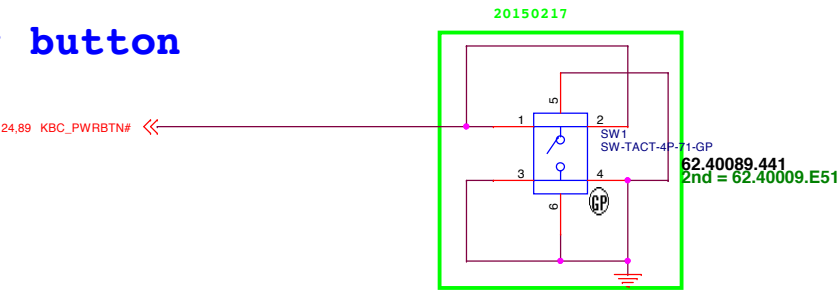
SSID = mSATA

per MP

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		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
mSTAT			
Size	Document Number		Rev
A3	Mihawk MB		-3
Date:	Tuesday, June 06, 2017		Sheet 63 of 105

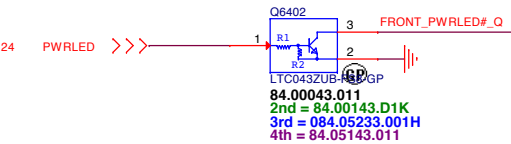
Main Func = Power BTN

Power button

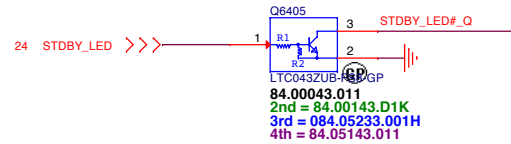


Main Func = Battery LED

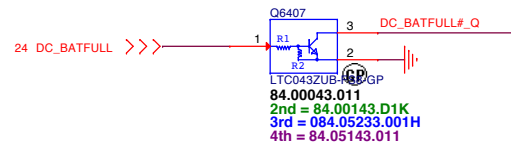
Power Button_LED



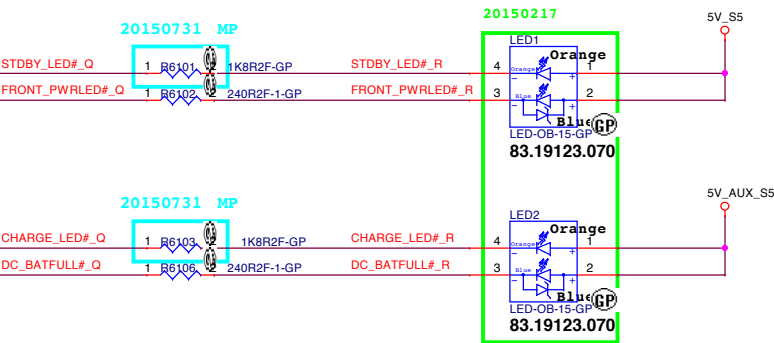
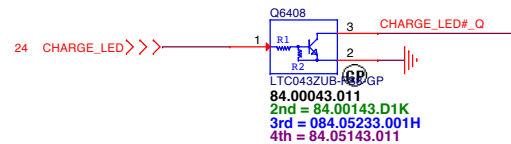
Power STDBY_LED



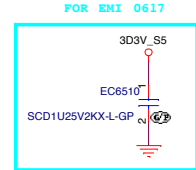
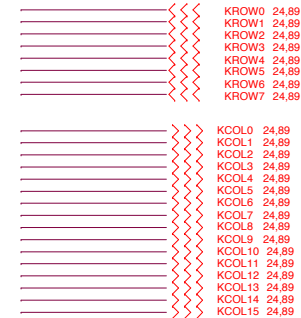
Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)



I2C Addr. = 0X2C (Synaptics)

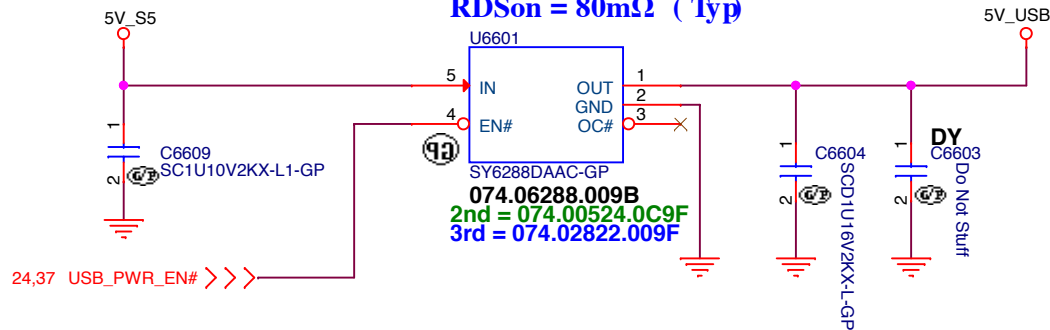
[illegible]

per MP

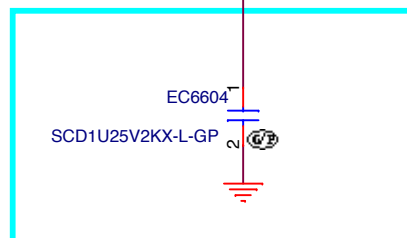
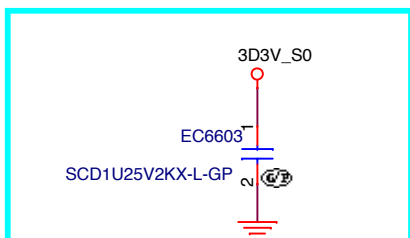
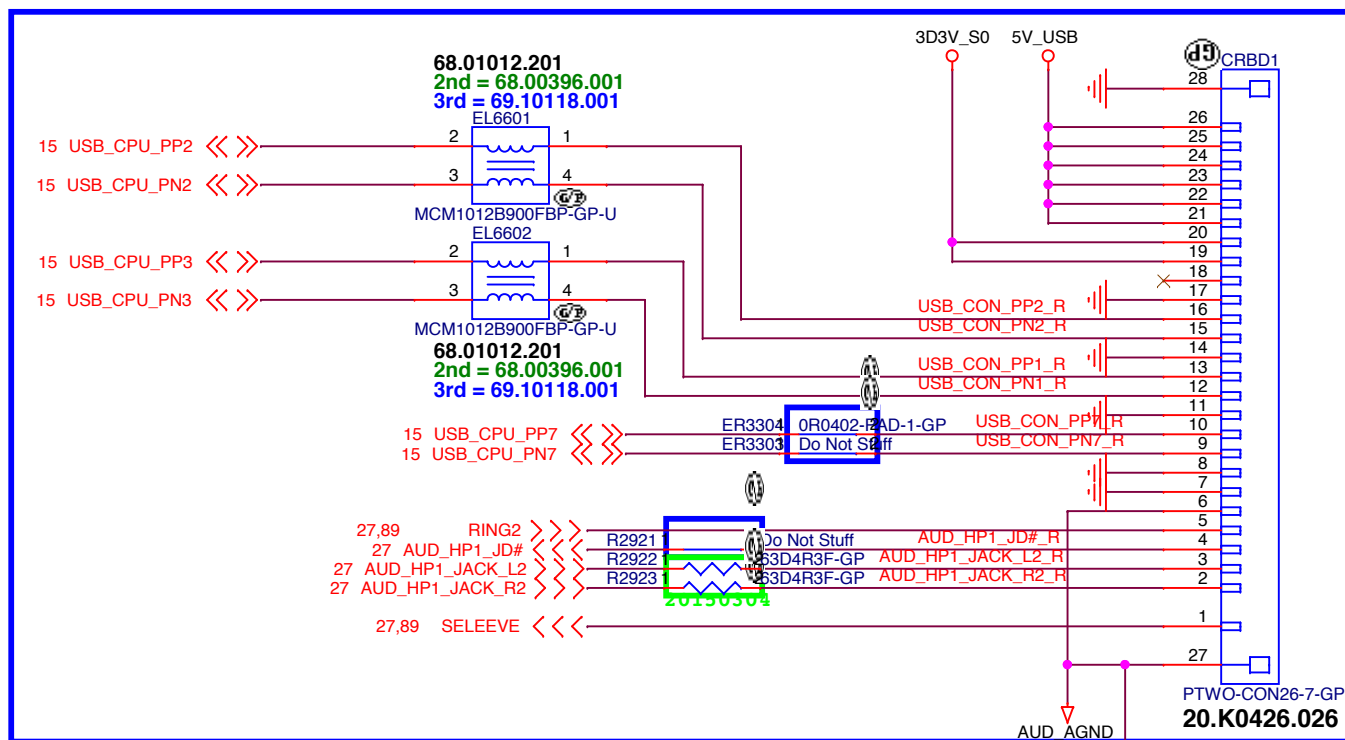
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Key Board/Touch Pad			
Size Custom	Document Number		Rev
	Mihawk MB		-3
Date:	Tuesday, June 06, 2017	Sheet 65 of 105	

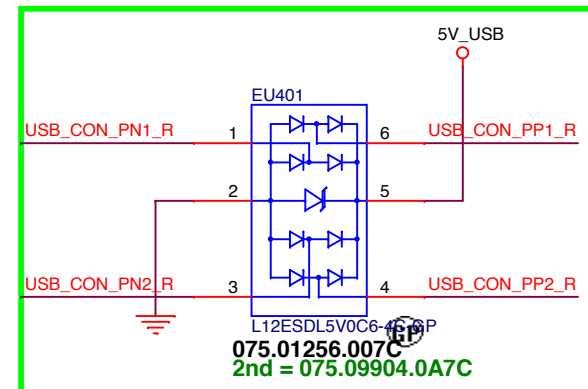
Low Active 2A
RDSon = 80mΩ (Typ)



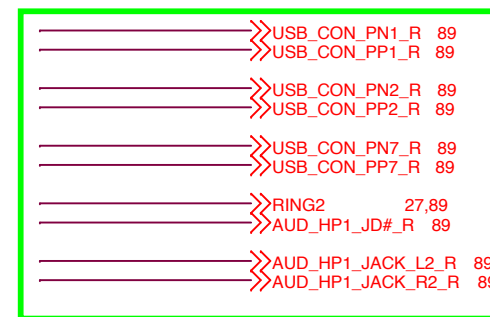
20150511 SB



20150331



20150310



AFTP TESTPOINT

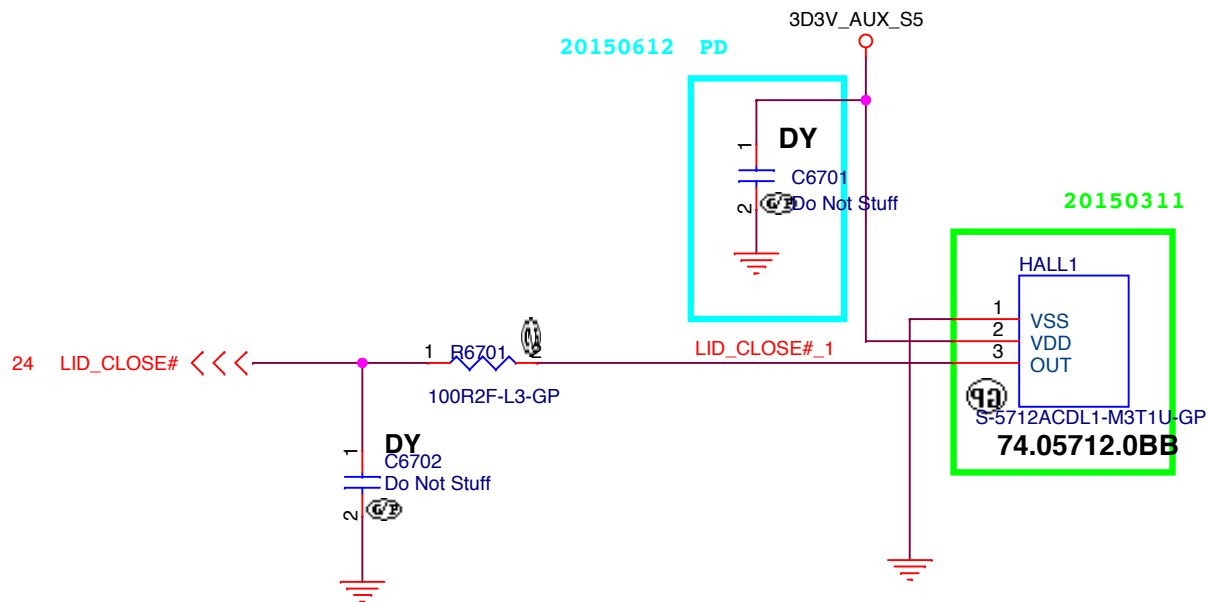
per MP

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Title **Key Board/Touch Pad**

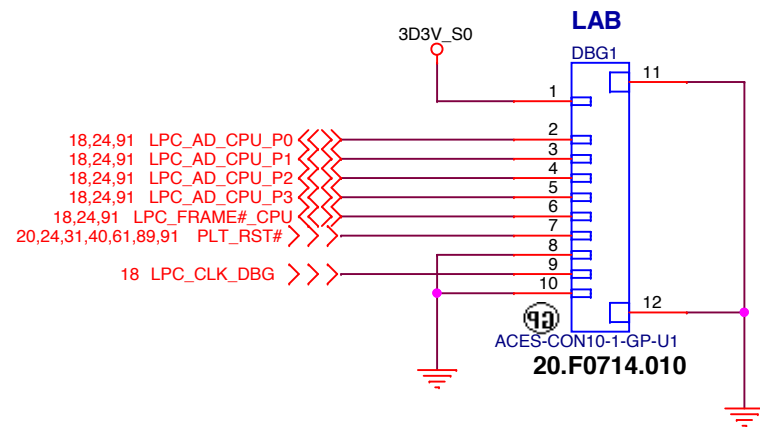
Size A4 Document Number **Mihawk MB** Rev **-3**

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Title Security Guard connector	
Size A	Document Number Mihawk MB
Date: Tuesday, June 06, 2017	Rev -3
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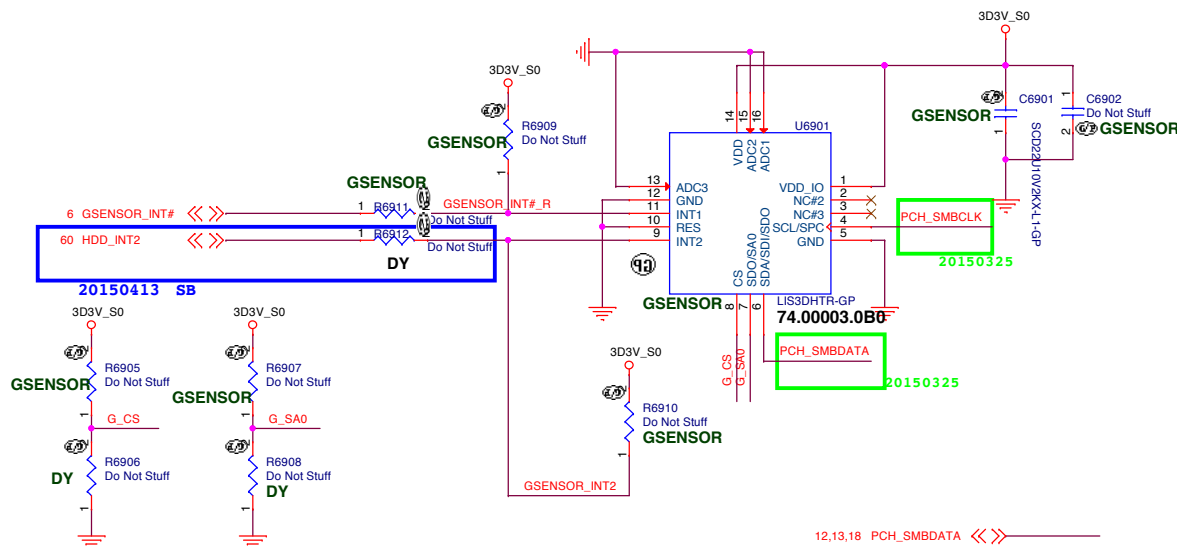


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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Dubug connector			
Size A4	Document Number Mihawk MB		Rev -3
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G Sensor

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



```
*CS="H"; mode="I2C"
CS="L"; mode="SPI"
```

12,13,18 PCH_SMBDATA <<>>_____

12,13,18 PCH_SMBCLK <<>>_____



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Title **Hall Sensor**

Size A3	Document Number Mihawk MB	Rev -3
Date: Tuesday, June 06, 2017		
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<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.</div>			
<div>Thunderbolt(1/5)</div>			
Title			
Size	Document Number	Rev	
A3	Mihawk MB	-3	
Date	198805, June 18, 2017	Sheet	71 of 156

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<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
TitleThunderbolt(2/5)	
Size A0	Document Number Mihawk MB
Date: 1080509, June 05, 2017	Rev -3
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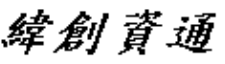
per MP

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>Thunderbolt(3/5)</div>	
Size A0	Document Number <div>Mihawk MB</div>
Date: <div>1080909, June 06, 2017</div>	Rev <div>-3</div>
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Title Thunderbolt (5/5)		
Size A4	Document Number Mihawk MB	Rev -3
Date: Tuesday, June 06, 2017		Sheet 75 of 105

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GPU (PEG)

Size
A2

Document Number
Mihawk MB

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Date: Tuesday, June 06, 2017

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5	4	3	2	1
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Title

GPU (DIGITALOUT)

Size
A3

Document Number
Mihawk MB

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Date: Tuesday, June 06, 2017

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Taipai Hsien 221, Taiwan, R.O.C.

Title

GPU (POWER/GND)

Size
No

Document Number

Rev

Issue

108209, June 06, 2017

Issue

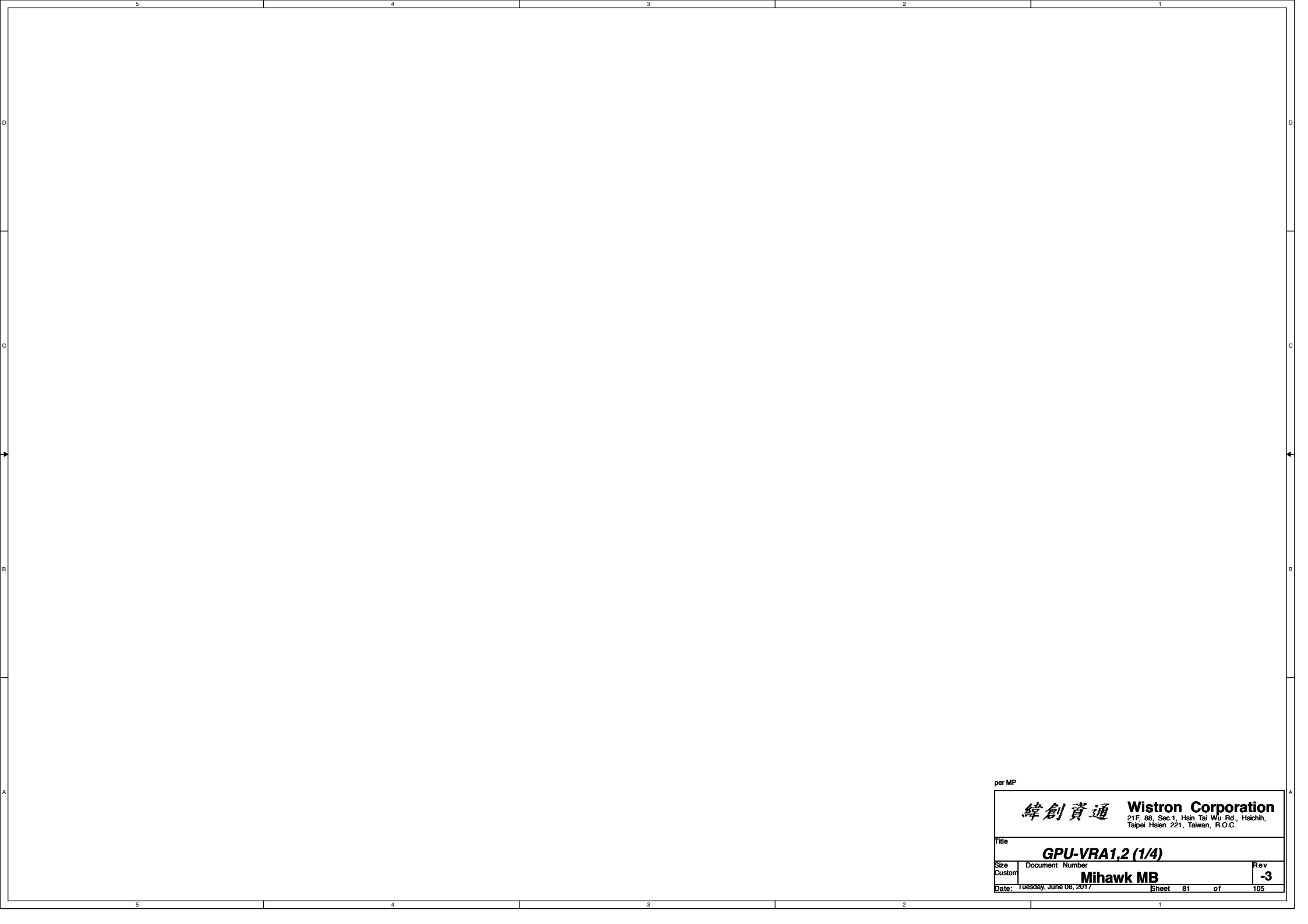
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GPU-VRA1,2 (1/4)			
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GPU-VRAM3,4 (2/4)			
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GPU-VRAM7,8 (4/4)			
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
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GPU-VRAM7,8 (4/4)

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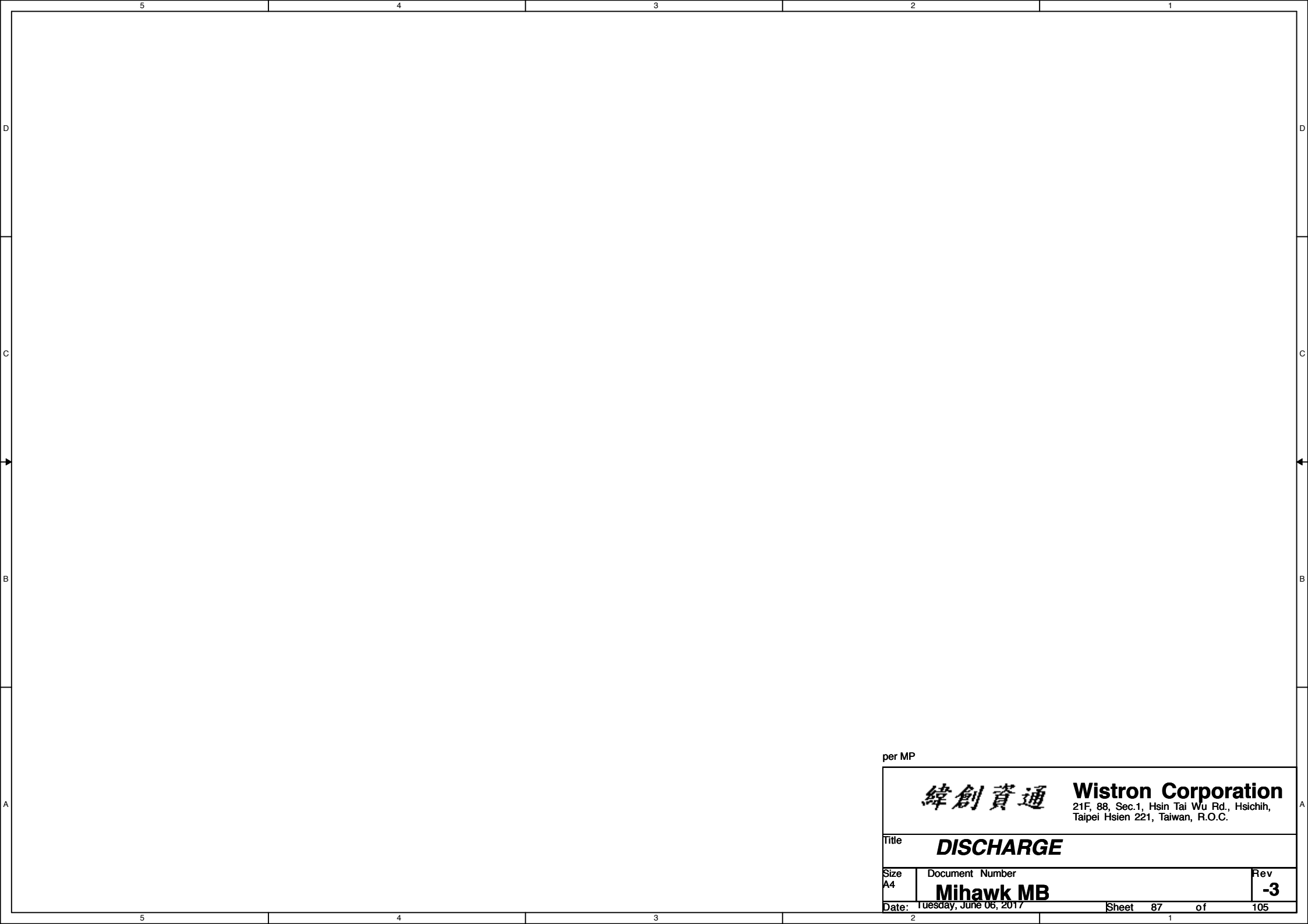
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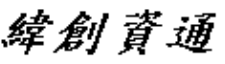
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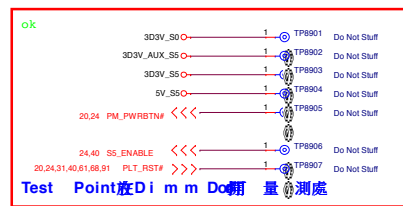
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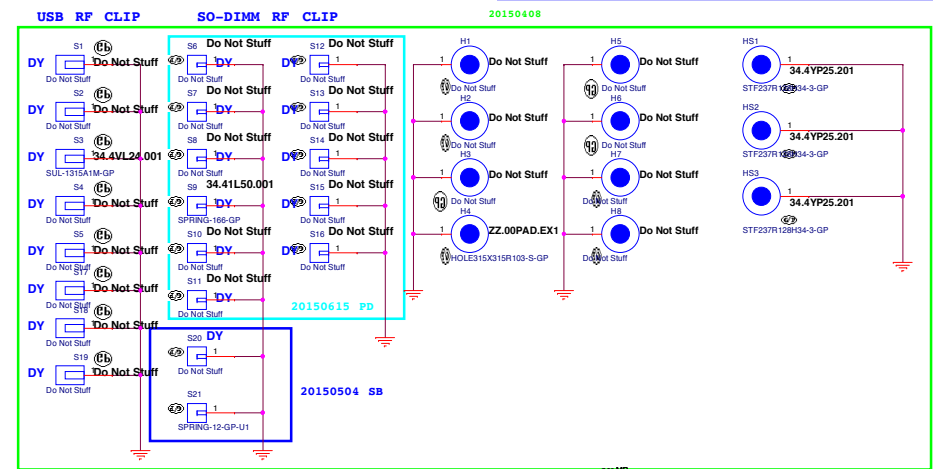
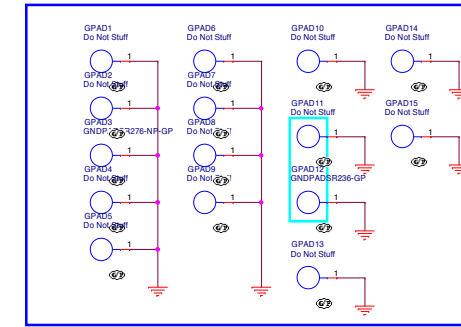
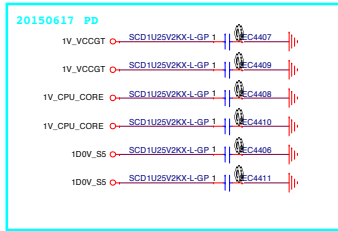
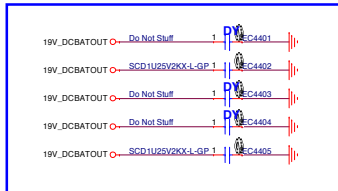
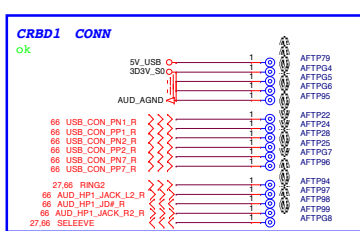
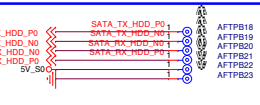
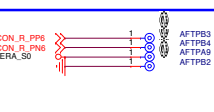
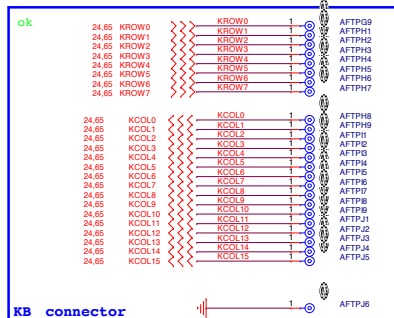
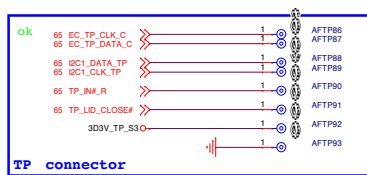
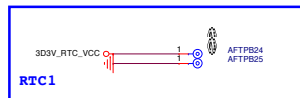
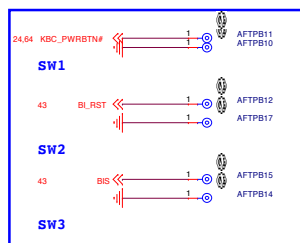
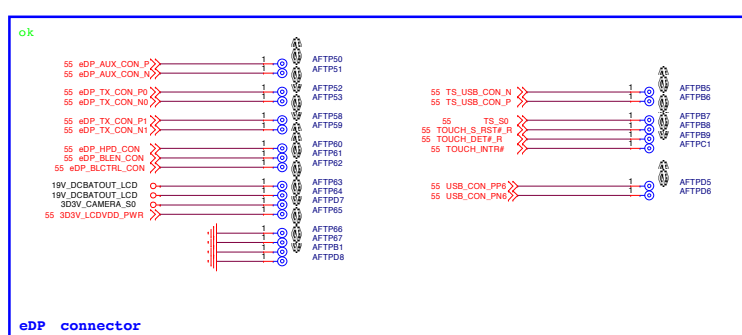
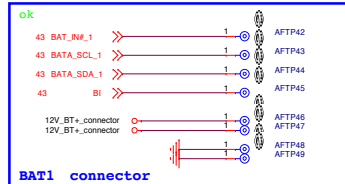
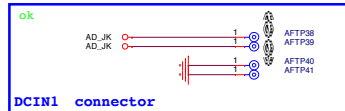
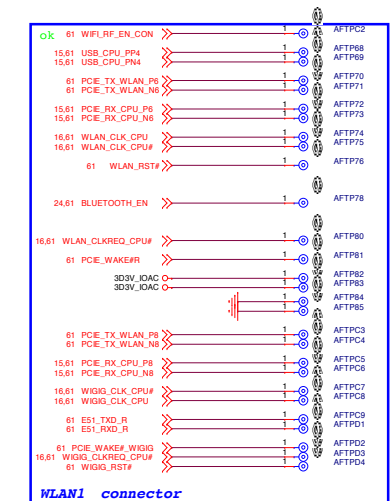
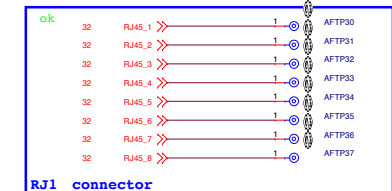
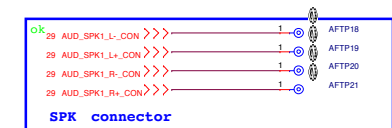
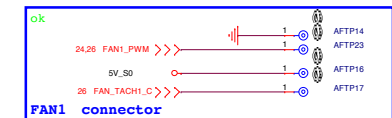
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Title Switchable GFX LCD(2/2)		
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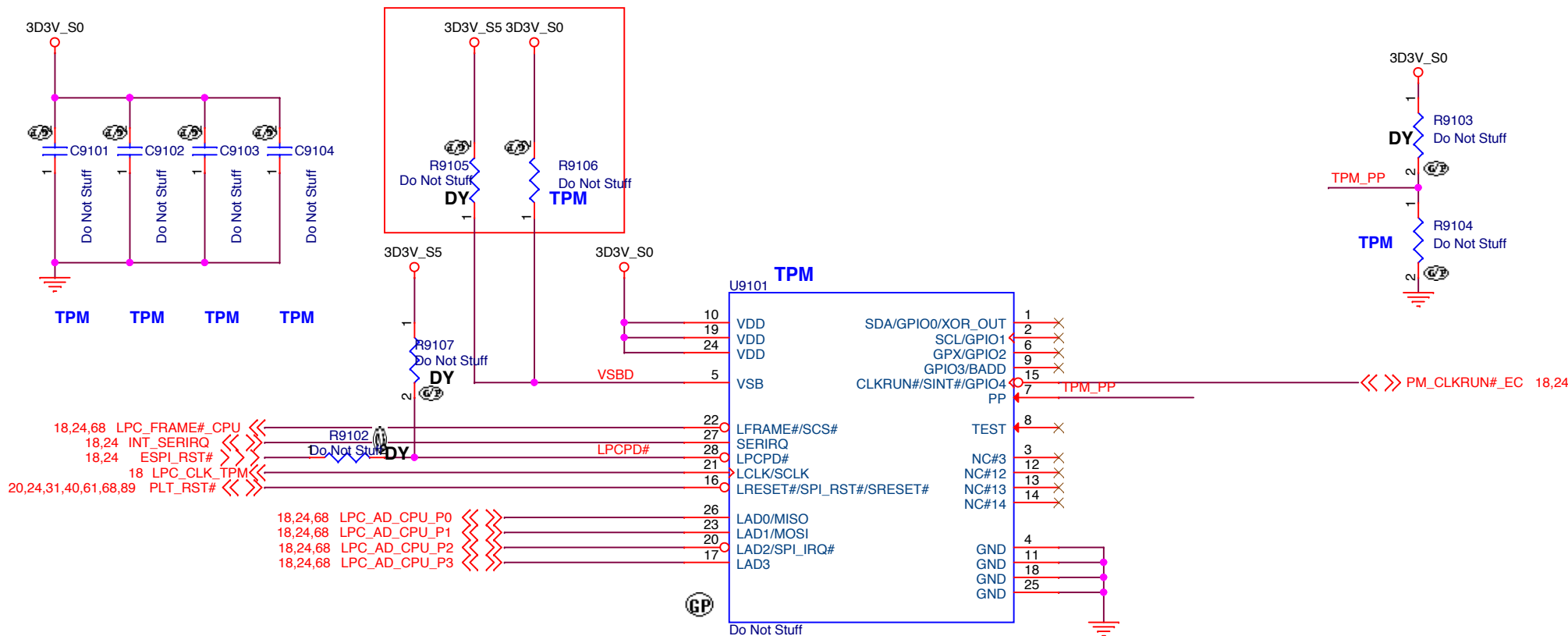


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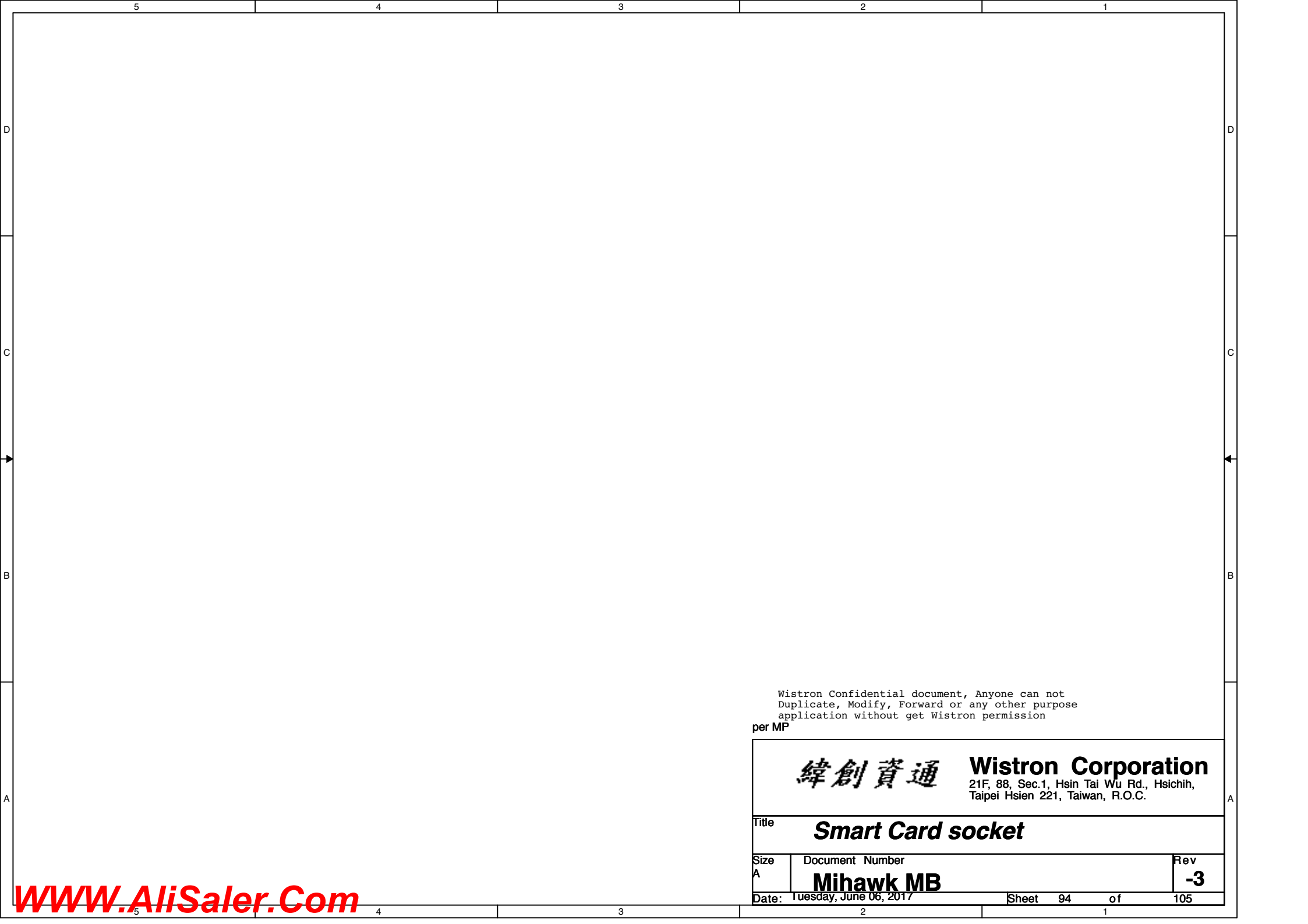
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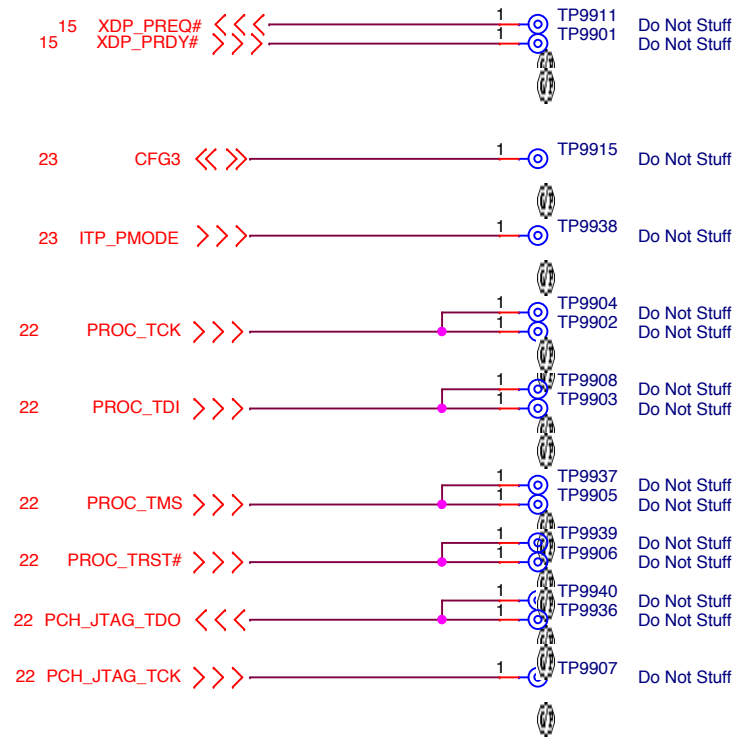
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Title **CPU_XDP**

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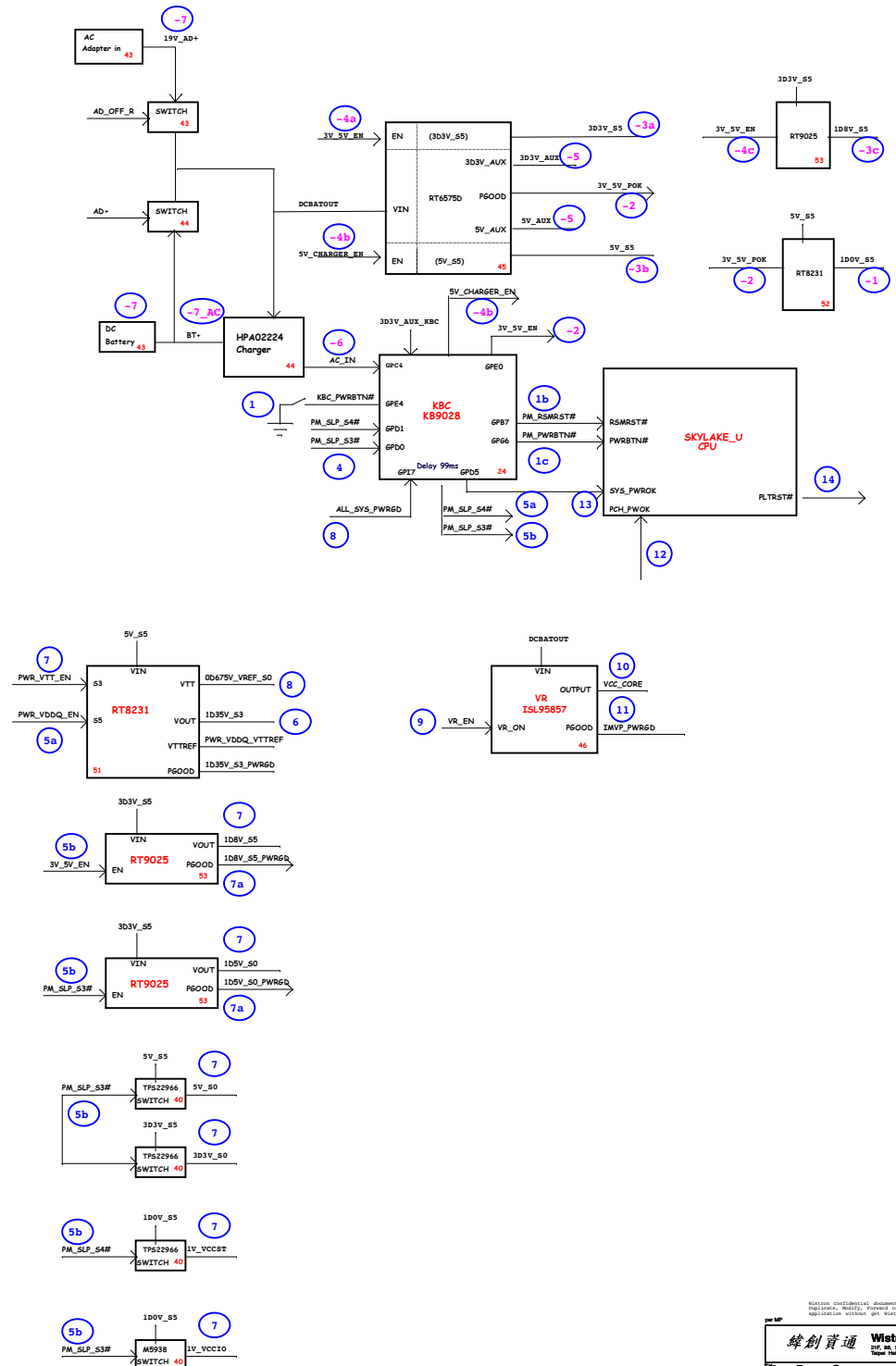
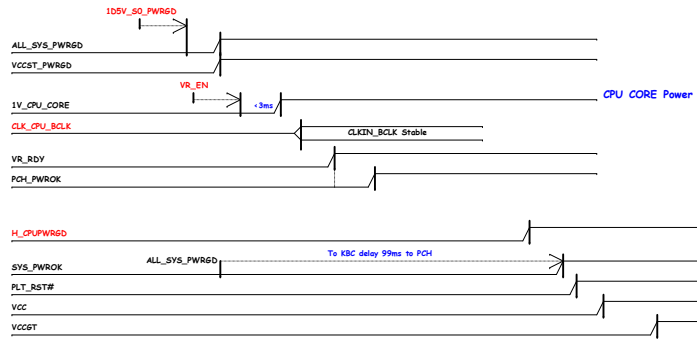
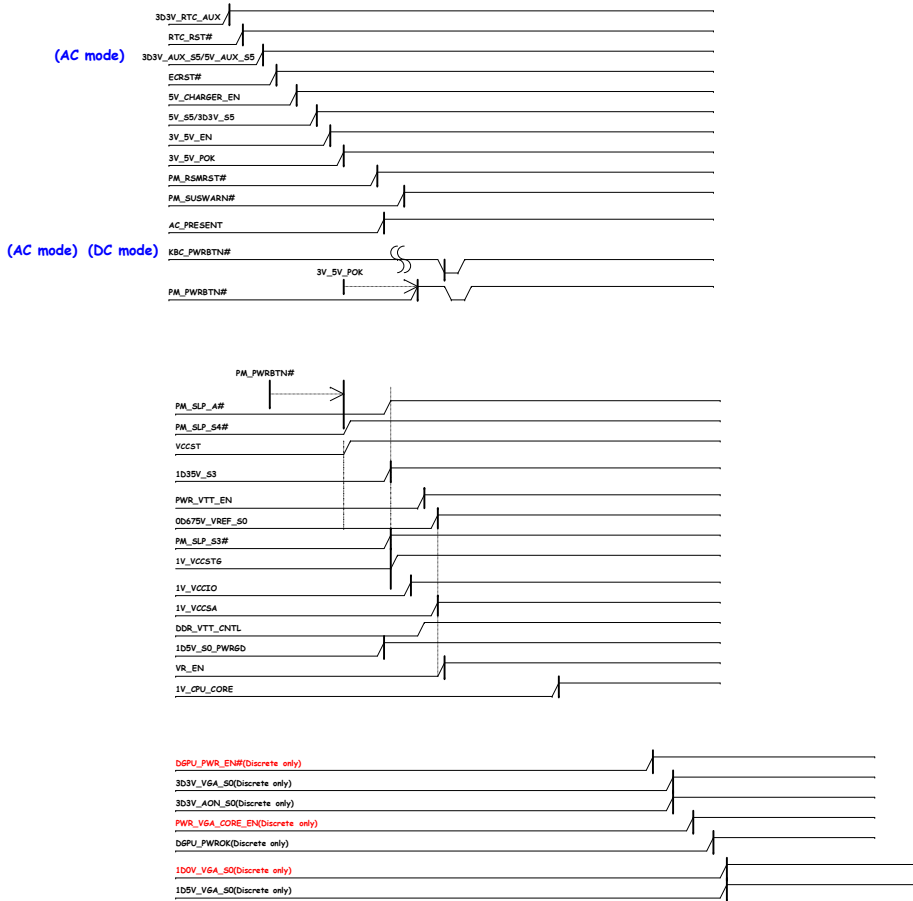
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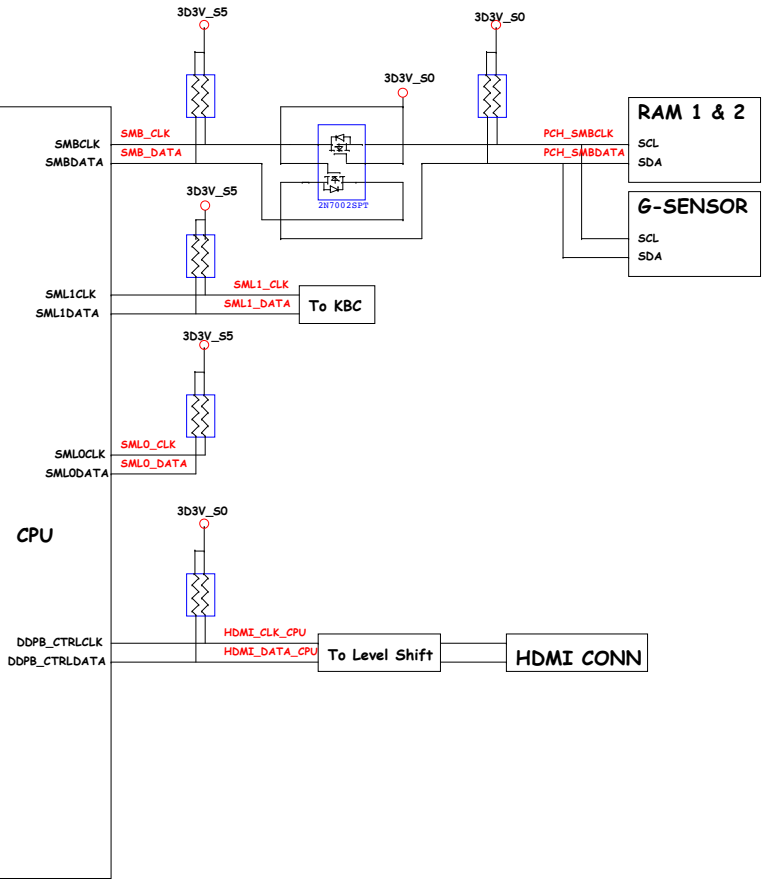
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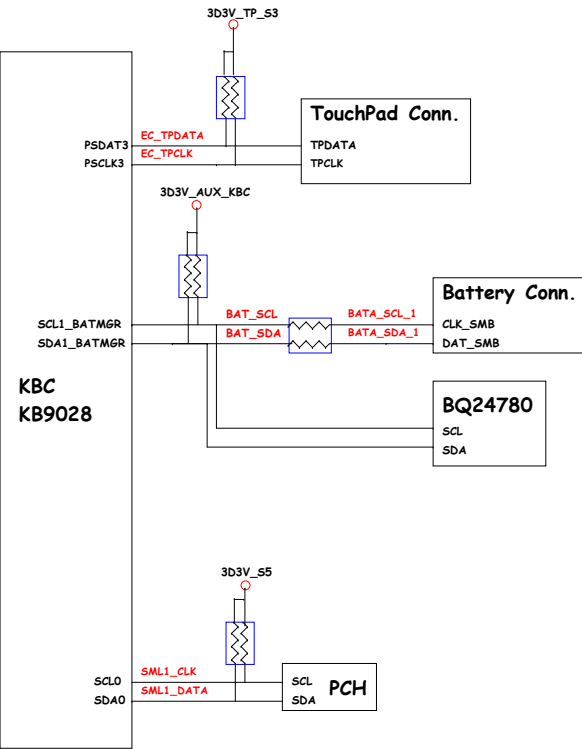
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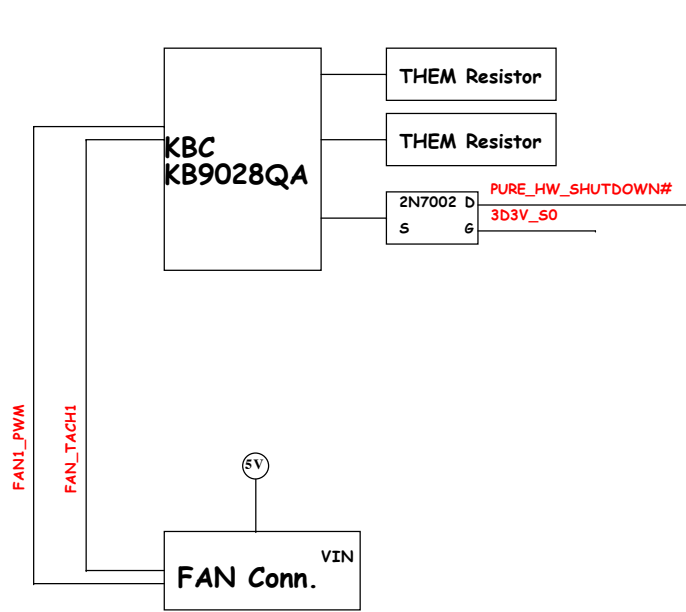
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KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

